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ANALOG DEVICES INC.

Ph.D.
THESIS

Viorel Bucur

REFERINTE DE TENSIUNE AVANSATE BAZATE PE DIODE ZENER

Advanced Zener-Based Voltage References

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Chapter 1

A Short History of the "Volt"

From the mid-19th century, a repeatable reference voltage standard was needed. Ideally, that standard reference cell would be a transportable device, insensitive to temperature variations, current flow requirements, aging related drift effects and it would have a long service life. It should also be possible for independent labs to construct the cell with a high degree of reproducibility. Due to technical limitations of the time, an electro-chemical voltaic cell was the initial obvious choice. The construction of such a device capable to meet most (ideally all) of these requirements was the subject of much research in the last 200 years.

1.2 A never-ending trade-off: precision (accuracy) vs. cost (financial or other nature)

Technical parameters listed as "**Key Specifications**" are usually the first reviewed by potential users when determining the suitability of a particular IC for a specific application. These parameters are considered critical by the manufacturer, therefore listed as such in the datasheet. A (non-exclusive) list of these specifications and their respective units of measurement for integrated voltage reference is presented below:

- Reference architecture (Each type has his own advantages & disadvantages).
- Voltage output values (Volt).
- Power supply (Voltage or Current requirements).
- Initial accuracy (% of FSR).
- Temperature functional range (°*C*).
- Temperature coefficient TC (*ppm/°C*).
- Full integrated IC chip (no external components).
- Reference output noise (u*Vp-p*).
- Device cost ($).
- IC Package availability (footprint & cost).

There are also a multitude of "**Secondary specifications**" which are critical performance parameters of the high-end performance portfolio of the Voltage References to be considered:

- Long Term Drift (LTD) (*ppm/1khr*).
- Post-reflow drift (Soldering on PCB) measured in ppm.
- Line regulation (*mV/V*).
- Temperature stabilised Silicon solution (directly linked to power supply requirements).

A trade-off would have to be made when determining the Primary and/or Secondary specifications importance priority in the design. Over constraining of these requirements could potentially result in an impossible design implementation and/or manufacturing task. The main focus of our investigation in this thesis will be on the temperature dependent IC packaged induced stress, TC, and hysteresis related variations of the reference output.

1.4 User orientated approach

Extensive research was performed in the current thesis, focusing on both key and secondary specification parameters of the industry "State of the Art" panoply of available voltage references ICs, regardless of the implementation principle. A detailed and comprehensive comparison (Table I) is identifying areas of strengths and weaknesses associated with each architecture. Both heated and hon-heated silicon-based voltage references architectures were included for completion in the research.

1.6 Thesis research objectives

The objective of this thesis is to improve the temperature overall performance of a precision silicon-based voltage reference, based on Zener diodes.

As presented earlier, mechanical package induced stress was identified as a major limiting factor of the overall modern IC performance [1]. The current research will attempt to reduce the plastic packaged influence in the ICs output voltage component, by utilising as our voltage reference a buried Zener device that is less susceptible to stress [2]. A innovative compensation method (named Flip ΔV_{BE}) based on ratio-metric voltages will be investigated. This is to be used as a replacement instead of the traditional forward biased diode [3], [4].

The thesis also presents a possible approach to obtain a Zener based reference voltage at a low supply voltage [5]. A charge-pump circuit will generate, from a low supply voltage, a higher output bias value. In the second stage, a low noise bias current is generated from the low voltage part of the proposed design, and then mirrored in the high voltage block, to supply current to the Zener diode. This way, stable reference Zener-based voltages can be obtained in terms of any value with supply from low voltages, between 2V to 5V.

A circuit consistent with this novel proposed compensation principle is designed, SPICE simulated and physically implemented in a standard manufacturing process. Assembled plastic packaged ICs are submitted to a full prototype evaluation cycle.

The final goal of this research is to produce a cost effective, package independent, **non-heated** silicon-based voltage reference with a **TC** in low single digits ppm figures (**ideally ~1ppm/°*C***) over the full temperature industrial range (**−55°*C* to 125°*C*)**. Simple, flexible & effective trimming circuit will also have to be developed for both the linear and nonlinearity components present in the reference output.

Investigating and mitigating all other thermal packaged related influences like **SHR**, **LTD** and hysteresis, which are directly impacting the final temperature IC performance, are particularly important to this thesis. Reducing the package induced stress of the n developed plastic ICs first, by the inherited resilience of the B-Zener diode and second by the innovative ratio metric ΔV_{BE} cell developed (less susceptible to mechanic / electrical stress), opens previously unchartered avenues for further research into the elusive 1ppm/°C temperature coefficient drift for a non-heated silicon-based voltage reference.

1.7 Brief thesis summary

As outlined in **Chapter 2**, there is no numerical model available for **B-Zener**, capable of describing accurately the device temperature dependency and the bias current implications of such. Device measurements were performed for both Zener devices utilised in this research. Based on a sample lot of **30 Zener diodes** for each devices type, results were utilised to build a numerical model for both the **S-Zener** and the **B-Zener** diodes temperature dependency for the full industrial temperature range. The novel developed model based on these measurements will allow to gain assurance with

a high degree of confidence that the simulation results will fit the silicon packaged die. Bias current influence in terms of both absolute value and temperature dependency variation will have to be investigated, as sources of nonlinearity errors.

Architecture and detailed circuit design, SPICE simulation, device analysis, layout implications and packaged IC measurements are all included in **Chapter 3** for our initial Test-Chip1 **TC1** architecture.

Highlights of Test-Chip1 (**TC1**) [6] performances (based 30 **PLCC** packaged ICs) are:

- **Non-Heated** silicon architecture (non-thermally stabilised).
- Low **TC** for all measured packaged ICs. **1ppm/°C <TC< 6.5ppm/°C**.
- Low supply voltage **(~5.6V** with **low $IDD = 100uA$**) for the initial design.
- Low Re-Flow drift <**400ppm.**
- Full industrial temperature range functionality: **−55°C to 125°C.**
- Low Long-term drift **(low digit ppm/°C** drift after 1k Hours).
- Reduced process dependency (Temperature compensation circuit is based on current **ratios of BJT** area which is less susceptible to drift).
- Easy and effective temperature coefficient **(TC) trimming.**
- **Plastic moulded package** (Low-cost alternative vs. expensive **TO-8 Metal**).
- Initial accuracy: **<1%** (No more VBE spread component).
- Small silicon footprint (less than **1sqmm**) and surface mount capabilities.

Based on packaged IC measurements performed on **TC1**, further enhancements will be extensively analysed, and a possible solution is proposed in **Chapter 4.** This novel architecture (named Test Chip 2-**TC2**) benefits from a reduced supply requirement **(Min 2.7V**) in the normal operating mode, while maintaining all other specification of **TC1** unaffected. As presented in **Chapter 4**, a charge-pump circuit will generate from a low supply voltage, a higher output bias value. In the second stage, a low noise bias current is generated from the low voltage part of the proposed design, and then mirrored in the high voltage block, to supply current to the Zener diode. This way, stable reference Zener-based voltages can be obtained in terms of any value with supply from low voltages, between 2V to 5V. Another highlight of the **TC2** die is the "Lego Like" modular approach that will enable us to perform an individual evaluation of the output components contributions. Based on plastic packaged **LFCSP** die, (**50 chip**) IC

measurements were performed on TC2. These have identified the **S-Zener** diode itself as a major limiting factor of the overall IC performance.

In **Chapter 5,** this research will mitigate the initial available **S-Zener** device with its limited performance and proposing an innovative architecture Test Chip 3 (**TC3),** including a high-performance **B-Zener** diode. A Co-Packaged B-Zener and associated compensation circuits are submitted to a full prototype evaluation cycle. Highlights of Test-Chip3 (**TC3**) performances (based on **100 QSOP packaged ICs**) are:

- **Non-Heated** silicon architecture (non-thermally stabilised).
- Low supply voltage **(~7.5V** with **low** $\boldsymbol{IDD = 100uA}$) for the initial design.
- Low TC for all measured ICs. **1ppm/°C <TC< 4ppm/°C.**
- Low **SHR** (Re-Flow) drift **<50ppm** (or +75% reduction vs. TC1).
- Initial accuracy: **<0.5%** (No more VBE spread component).

All other parameters were unaffected by this enhancement and have remained the same as per the **TC1** chip specifications.

In **Chapter 6,** a novel Patent (pending) for a nonlinearity correction method is developed. To expedite the Patent application, a stand-alone correction circuit for an ultra-precise temperature sensor is proposed. This innovative correction method can be incorporated into the current flip ΔV_{BE} compensation circuit described in **Chapter 3** (similar with patent functionality) and it facilitates the Zener-based reference design nonlinearity correction. This proposed correction circuit is currently undergoing a full detailed analysis of circuit design, SPICE simulation, mismatch analysis, layout implications and packaged ICs capabilities.

Finally, conclusions will be drawn while establishing to what degree our initial research goals were achieved and possible areas where further research investigations are required. As our goal is to manufacture a cost effective, package independent, non-heated silicon-based voltage reference with enhanced performance, all the remaining measurements associated with a full prototype evaluation cycle will have to be finalised to guarantee product specifications compliance.

Chapter 2

The Zener Diode Model

Most of the simulation models available to date are of the discrete Zener diodes standalone components [7]. A novel model for an embedded Zener diode will be required in order to perform all the simulation and verification portfolio tasks before the actual TC1 chip manufacturing. There is a lack of detailed Zener device solid state physics analysis and mathematical support when one is discussing a functional device implementation associated with a "real" Zener diode behaviour.

Being able to access these PSpice spice model databases for discrete complements [7] is a valuable tool at one's disposal. ROHM Semiconductor is providing a large collection of discrete Zener diodes models, with Zener voltage varying from **3.6V** to **36V**, for academic and no-commercial use [8]. These Zener models were used as a numerical model starting point in analysing our own embedded Zener device temperature dependency characteristics.

Based on the analysis, a numerical model is proposed having the following terms: absolute value, linear and nonlinear components as described in equation (2.1):

$$V_z = V_0 + \alpha \frac{T}{T_0} + \beta T \, ln\left(\frac{T}{T_0}\right) \tag{2.1}$$

where: V_Z= overall Zener voltage temperature dependency, $\boldsymbol{V_0}$= temperature independent value associated with extrapolated Zener value at 0K, $\boldsymbol{\alpha}$ coefficient associated with linear temperature dependency, $\boldsymbol{\beta}$ coefficient associated with non-linear temperature dependency in the form $T\,ln(T)$.

Due to the constraints presented earlier, a black box measurement approach will be implemented in this thesis. Measuring and analysing the uncompensated Zener voltage will be performed from the temperature dependency output variation point of view. Based on these measured values, a novel temperature dependency mathematical model will be proposed for both the embedded Surface and Buried Zener diodes.

The nonlinearity associated with this uncompensated Zener voltage will be measured, analysed, and simulated especially from the bias type of temperature dependency currents point of view (i.e., **PTAT, ZTAT, CTAT**). Ultimately, in order to achieve the desired single digit ppm temperature coefficient of the reference voltage this nonlinearity will have to be controlled, even compensated, and user trimmable circuits made available post manufacturing. The absolute value and temperature dependency of the biasing current induce a variation in the uncompensated Zener voltage output value. The ability to decouple the nonlinearity bias induced component from the compensated reference voltage is a powerful one. Any bias current can be selected as required by the design specifications and the inherited induced nonlinearity can then be compensated. A possible compensation methodology applicable in this case is presented in the current thesis [9] and captured in **Patent Application APD6917US01** "A Circuit for Generating a Temperature Dependent Output" (filed January 2020).

Chapter 3

IC TUCBZ Architecture

3.1 Flip Delta V_{BE} cell (ΔV_{BE})

As presented in Chapter 1, the temperature insensitive voltage references can be divided into two main categories: Buried Zener type and Bandgap voltage type [10], [6]. Both have advantages and disadvantages. Reference voltages based on buried Zener are less sensitive to stress and have lower LTD (approx. 3ppm/1kh) [3], [6]. Their main drawback is related to the minimum supply voltage, of at least 6.5V. Bandgap-type voltage references can operate off supply voltages as low as 1V, but they have larger LTD compared to Buried Zener type (**typically <30ppm/1kh**) [11], [6].

The uncompensated buried Zener voltage has a typical **TC** of about **+2mV/°C** (value for a **6.3V** Zener diode at **27°C**) [12], [6], as presented in Figure 1.6. Embedding in the new architecture a digital control TC compensation circuit is desirable and is enhancing

the flexibility and **TC** performance of the innovative design. Traditionally [3], [6] this temperature dependency is compensated by adding to the Zener voltage a base-emitter voltage of a forward-biased bipolar-junction transistor which has a **TC** of about **+2mV/°C** [13], [6]. The overall result is a quasi-flat TC characteristic, but the two voltages are never perfectly balanced [14], [6]. Furthermore, by maintaining the Co-Packaged Zener and compensation BJT at a stable, user selectable forced controlled temperature, significantly higher than the ambient temperature, the temperature dependency of the Heated Based B-Zener voltage reference is eliminated.

Based on our previous Zener model presented in **Chapter 2**, by using the proposed flip ΔV_{BE} cell the linear temperature term $(\frac{T}{T_0})$ is reduced as presented in Equation 2.1, practically eliminating it. With careful design, the only remaining temperature dependant term is the non-linear one $(\frac{k \cdot T}{q} \ln\left(\frac{T}{T_0}\right))$, as discussed **Chapter 2**. At this stage of our investigation, the plan of action is to reduce the nonlinear term by selecting the appropriate bias current absolute value and temperature dependency accordingly. The new architecture does not use the uncontrolled process dependent V_{BE} ($\boldsymbol{CTAT}$) [14], [6], to compensate a Zener diode **(PTAT)** [12], [6]. In contrast with the classical architecture [3], [6], a V_{BE}($\boldsymbol{CTAT}$) voltage is not added to a Zener diode **(PTAT)** voltage, but is subtracting a ΔV_{BE} ($\boldsymbol{PTAT}$) from it, as shown in Figure 3.1 [15], [6].

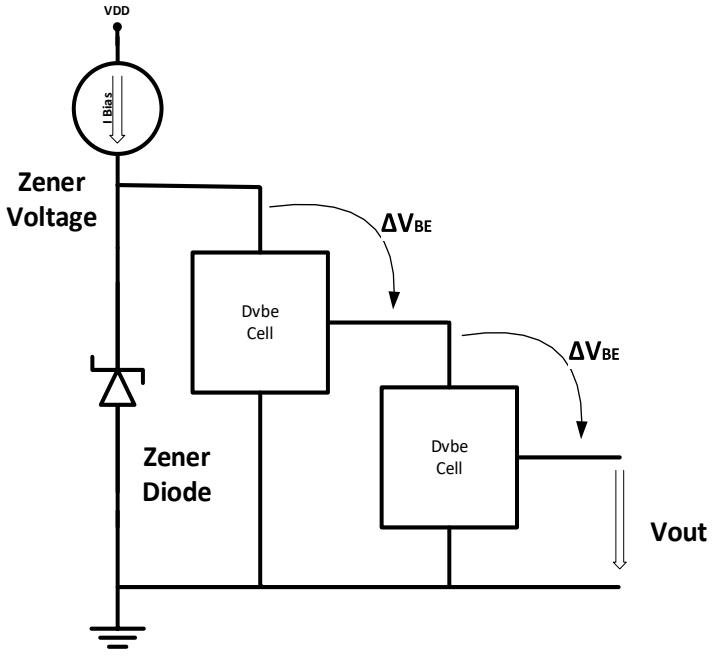

Figure 3.1 Innovative Zener-TC1 architecture block diagram

Starting with Prof. Dr. Stefan Marinca's original USA patent **US8531169B2** [16], a novel cell topology is developed, suitable for our requirements. The innovative concept is that to generate the required compensation (PTAT) voltage as a drop from VDD, or a non-heated Zener uncompensated voltage and not as a voltage from ground up as proposed in the original patent proposed circuit.

3.6 TC1 physical design implementation details

A **0.6µm Bi-CMOS** Analog Devices proprietary process was selected for the physical implementation. This high performance/low-cost technology node was selected as it has already supported and modelled all the necessary components required in the current design: PNP BJT, NPN BJT, Zener Diodes, Rectifier Diodes, LVNMOS, HV NMOS, 5V PMOS, 5V NMOS, NWCAP, Poly-Poly Caps, TFR Resisters. TC1 was laid out in a typical test chip configuration.

3.7 TC1 IC packaged evaluation

The compensated output voltage (Vout-Zener) was measured using the Agilent 3458A, and the Idd was measured using the Keithley 2000 multi-meter. Preliminary results recorded at **25°C** were very promising with a standard deviation of **9.31mV** and a mean value of **4.786V**, as shown in Figure 3.26 [2], [6].

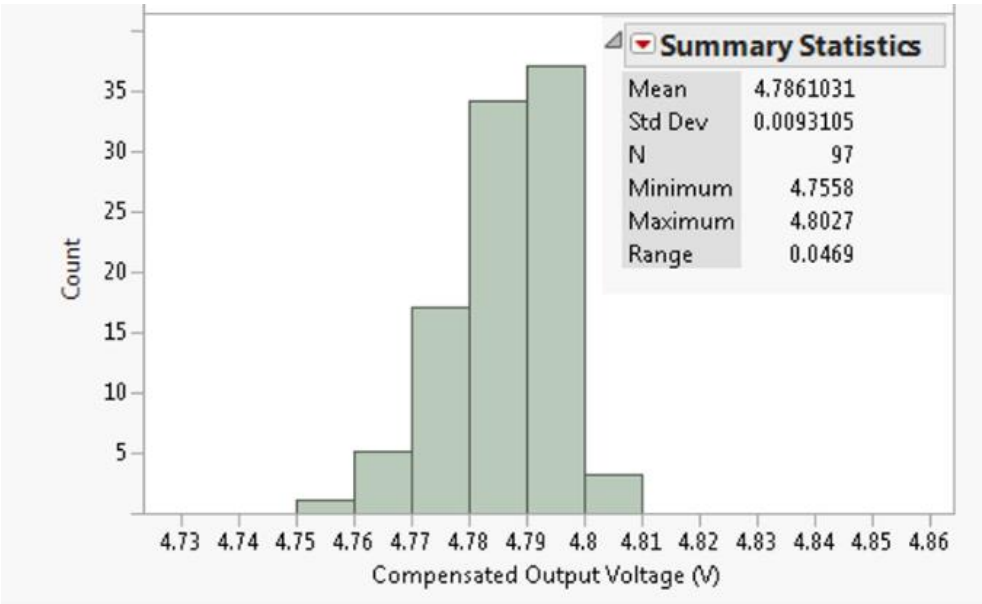

Figure 3.26 Measured standard deviation at 25°C of 9.31mV, and a mean value of 4.786V

Based on these **97** samples an initial accuracy of **<1%**, for six sigma distribution was calculated. A temperature coefficient was calculated for a selection of tested parts, after trimming of less than **1.5ppm/°C**, as shown in Table II. The trimming codes required for best TC are very similar to the predicted values (middle of trimming scale) and they confirm a good parameter correlation between simulation and silicon results [2].

Trimming range and functionality checks were performed with promising results.100% functional dies were observed out of the **97 parts** that were functional at the initial testing stage. Being able to measure and correct both positive and negative TC of the Zener diode proves that the correction sign presented in Figure 3.28 performed as intended in the design.

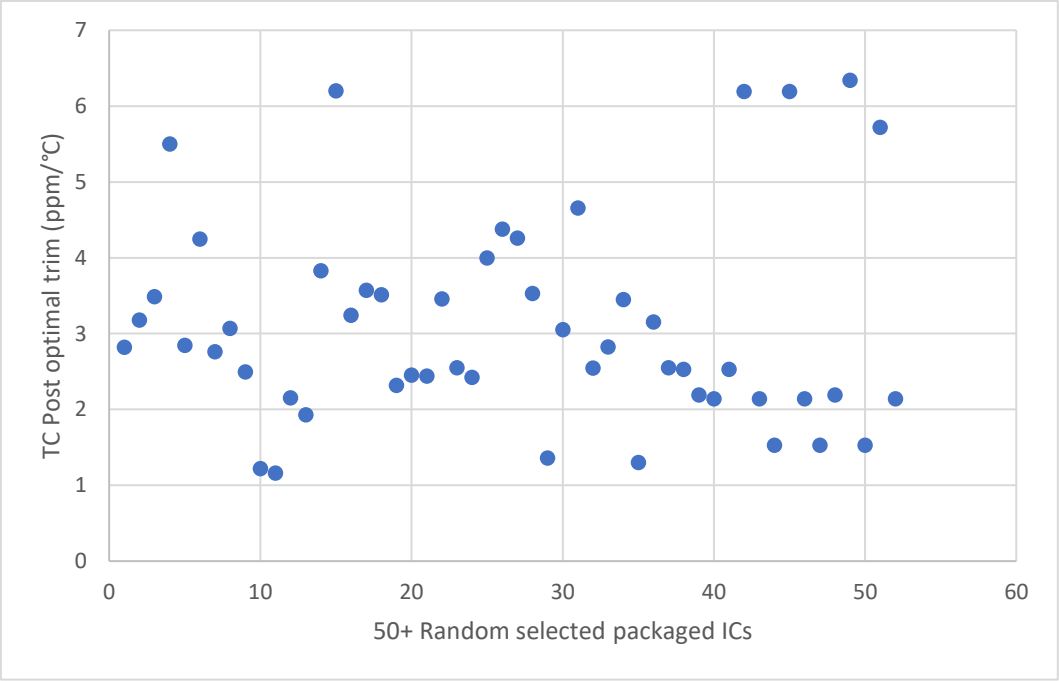

Figure 3.28 TC measured for 50+ Random selected parts

The formula used to calculate these TC values was as follows:

$$TC = \frac{(\Delta V * 10^6)}{V_{@25°C} * \Delta T} \tag{3.8}$$

where ΔV is the difference between Vmax and Vmin, ΔT is the temperature and $V_{@25°C}$ is the reference voltage at **25°C**. For the best trim codes for each device, a comprehensive picture of the **TC** measured for the **50 random** selected parts is presented in Figure 3.29.

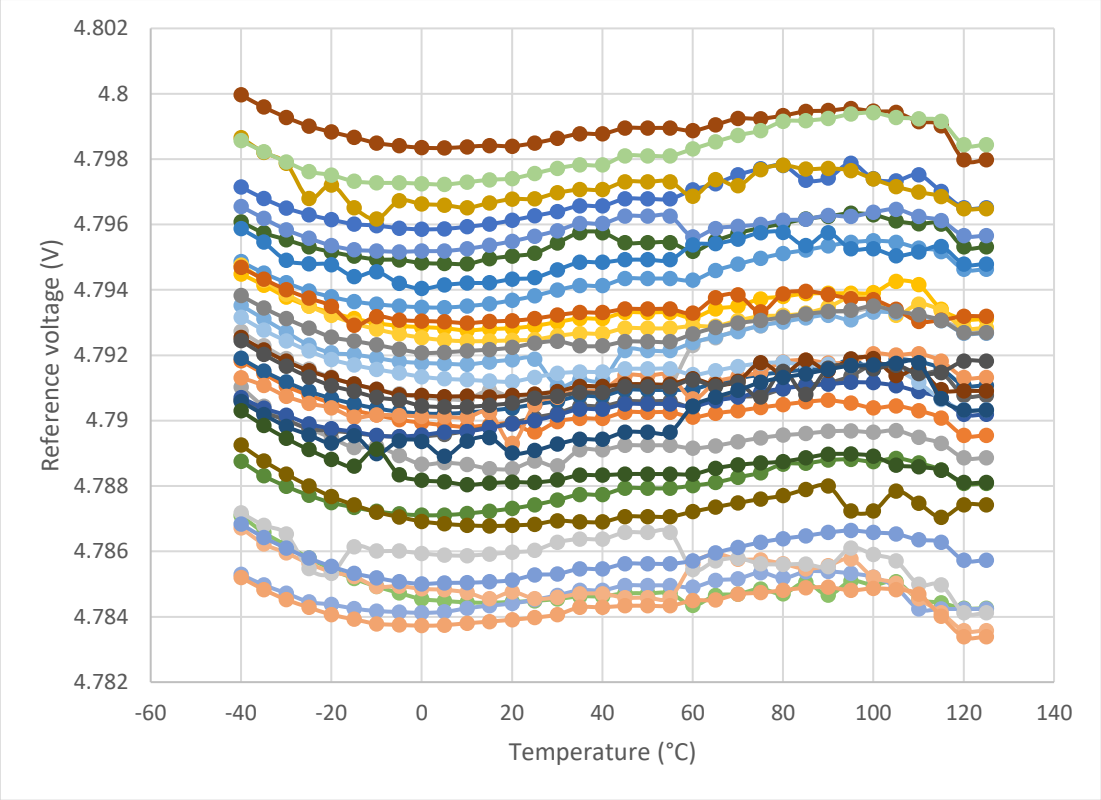

Figure 3.29 Output reference voltage vs. temp for all measured devices

By removing some outline devices, the compensated reference voltage vs. temperature post optimal trim for all the measured parts, is presented in *Table II.*

Table II. Best trim codes and their corresponding TC values, **[6].**

DEVICE	BEST TRIM CODE	TC (ppm/°C)	Vref @27°C
1	trim code 7 (0111)	1.36	4.794
2	trim code 8 (1000)	1.45	4.786
3	trim code 9 (1001)	1.23	4.786
4	trim code 7 (0111)	1.16	4.784
5	trim code 7 (0111)	1.3	4.783
6	trim code 10 (1010)	1.22	4.781

By design, the innovative proposed architecture is generating the value of the ΔV_{BE} voltage drop as a BJT area ratios, as explained in Chapter 3.1.1. Also availing of the flexibility of the novel proposed circuit, identical biasing currents $I2 = I3$ are used in order to reduce the impact of the first order effects on the output voltage as shown in Figure 3.28.

Chapter 4

Lowering TC1 supply voltage

4.1 Front-end Charge-Pump

The innovative proposed architecture Based on **Non-Heated Zener Diode**, named **TC1** has retained or improved most of the Heated Silicon Zener-Based Voltage References performances, from the **Initial Accuracy**, **TC, LTD** and **Re-Flow** point of view but is also suffering the limitation of a Zener-Based Voltage Reference in the form of the minimum input voltage requirements of **~ 5.6 Volts**. In order to mitigate this limiting factor a Charge Pump front-end used to reduce the power supply requirements to approximately **2.5 Volts**, while maintaining other design parameters unaffected. A modular "**LEGO-like**" approach design architecture will be implemented, allowing us to separate the nonlinearity components of each individual block contribution in the overall output voltage reference. An innovative current biasing circuit will be designed in order to reduce the chopping noise associated with the CP. Noise reduction specific layout techniques will be used in the sub-blocks themselves and a special trench isolation will be deployed to separate the CP block from the embedded reference area of the die. Not as efficient as separate die but cost effective, this technique will minimise the overall disturbance induced in the output reference voltage by the CP block itself.

4.1.2 Charge-Pump performance and ripple attenuation efficiency

Extensive simulations were performed to validate the proposed architecture. Desired power supply range is VDD **3V** to **3.6V** with a nominal value of **3.3V**. Simulation showed that the proposed design operates within parameters even when connected to a voltage source as low as **2.7V**. Under full load and with VDD set to **3V** as per the lowest power supply requirements specification, the maximum start-up time was found to be **70us** at **-40°C** under all process corners as presented in Figure 4.7.

The start-up time increased by less than 10% after adding the parasitic ***RC*** extracted from the layout into the simulation. The ripple at the output of the RC filter was attenuated from v_{CP}=**88mV** to a value of v_{RC}=0.**05mV** or by **66dB** as per Figure 4.7. The overall influence of the CP voltage ripple on the Zener reference voltage V_{Zener} was simulated at $\boldsymbol{V_{Zener}}$**=0.2uV** or approx. **112dB** reduction versus initial CP voltage ripple output. Furthermore, the $\Delta\mathbf{V_{BE}}$ [6] circuits would act as ripple attenuators themselves, and the overall voltage ripple component in the output reference voltage was simulated at **0.07uV** (v_{REF} of **4.75V**) or **125dB** ripple attenuation compared to CP voltage output ripple vCP.

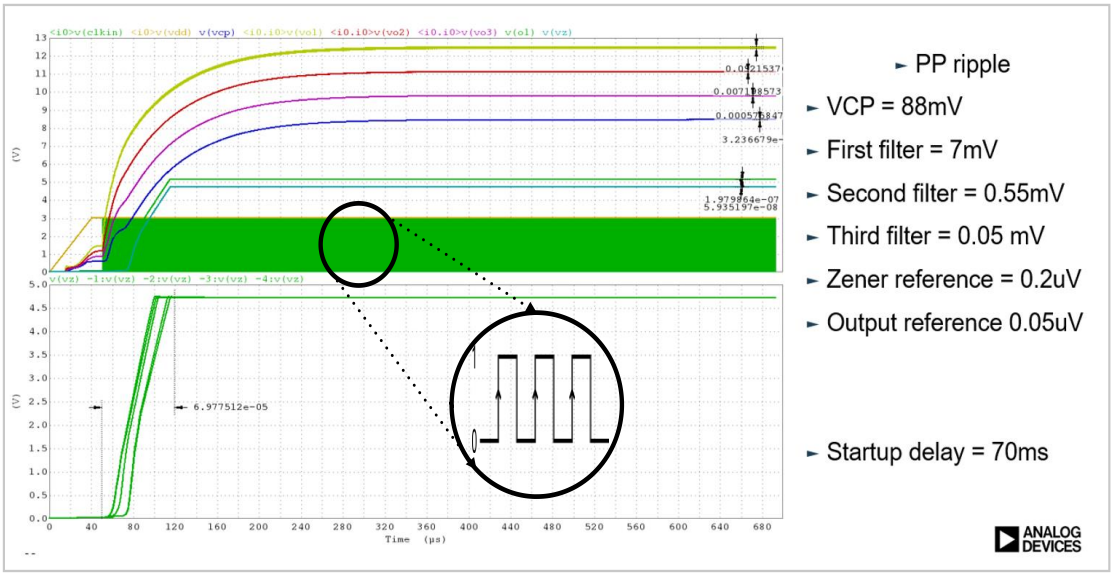

Figure 4.7 Start-up delay and CP output ripple attenuation

Finally, after adding the parasitic RC extracted from the layout into the main simulation, the ripple propagated to the output reference voltage was of a similar magnitude as the non-parasitic one as presented Figure 4.1. This ripple simulated value is at least **10 times lower** when compared with the best Zener-based voltage reference available [17].

4.2 TC2 physical design implementation details

The existing test chip was implemented using Analog Devices, Inc. proprietary 0.6µm Bi-CMOS 16V HV process. As the process had all the required components i.e. Schottky diodes, low leakage Poly-Poly capacitors available as standard devices, as well as high density HV-Nwell capacitors and also complementary PNP & NPN BJT

required for the ΔV_{BE} correction circuit, it was our obvious choice for the CP test chip design.

Attention to details was required in order to minimize the noise leakage into the adjacent circuits. A P-diffusion, Deep N-well, P-diffusion trench isolation is used to separate the two parts of the circuit: on one side the noisy switching part of the CP and associated support circuits, and on the other side the quiet area of the Zener diode and the ΔV_{BE} compensation blocks. The switching elements, i.e., Schottky diodes, were physically placed on silicon as far as possible from the sensitive differential input pairs of the PTAT current generator. Individual tracks of low resistivity were used for each of the blocks to minimize noise coupling in-between functional blocks. Most of the CAD layout good practice techniques such as resistor, bipolar and diodes dummies were used in order to improve the matching as per norm in the development of the **TC2** test chip. [18] Adequate substrate diffusion was used to minimize substrate leakage and reduce noise coupling. The power and ground tracks associated with the noisy part of the die were separated from the quiet zone area of the layout. Power and ground rails are connected to separate pads for each functional block of the circuit.

These pads are individually bonded in the package to minimize interference. Both the power and ground tracks maintain low resistivity values from the pad to the circuit blocks to provide good isolation and minimize noise coupling [18]. The overall area of the test chip is approx. **2.4** $\boldsymbol{mm^2}$ including the ESD protection of the pads. The **CP** and the **RC** filter occupy approx. **0.75**$\boldsymbol{mm^2}$, the **PTAT** quiet generator and the Low & High Current Generators including the ΔV_{BE} cell are occupying approx. **0.75** $\boldsymbol{mm^2}$. The rest of the **0.75** $\boldsymbol{mm^2}$ is occupied by the ESD pad protection and the extra isolation trench.

4.3 TC2 IC packaged die evaluation

Identical equipment (except a new PCB board), method and procedures were used for **TC2** as ones used and described for **TC1** in **Chapter 3.4**. The only difference was the **LFQSP** IC package selected for TC2 to be able to accommodate a larger die footprint and a larger number of bonding pads required. Bonding diagram for the original developed TC2 and the associated die image are presented in Figure 4.11.

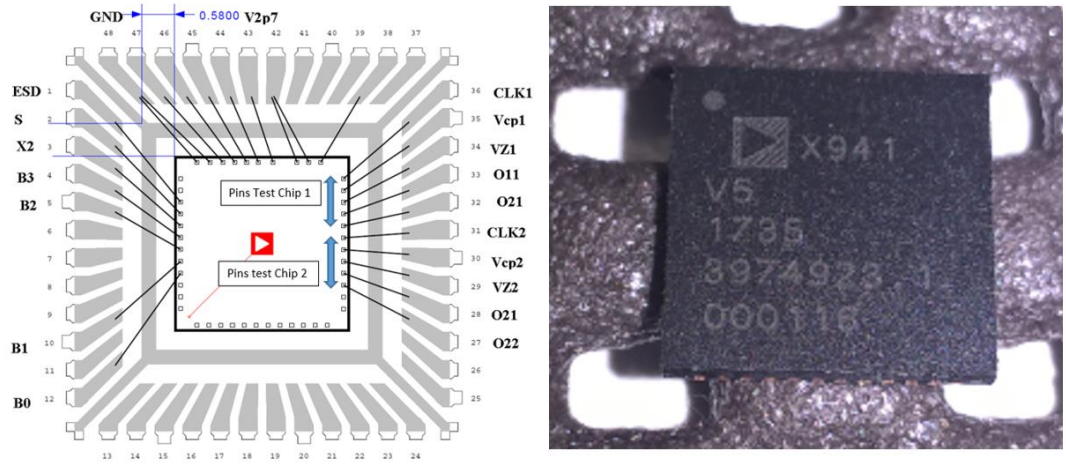

Figure 4.11 Zener-TC2 bonding diagram and LFCSP die view

Modular approach was employed in the TC2 design in order to reduce further development time, help with fault and errors identification. As a positive implication of this modularity, individual contribution of the building blocks was available for detailed analysis as per **Chapter 4.3.1**.

All major blocks were decoupled to facilitate a "LEGO-like" fast debugging and developing technique. Access points, marked in green, accessible to the outside world are presented in the Figure 4.12 (from the schematic point of view) and Figure 4.13 (from the layout point of view) respectively.

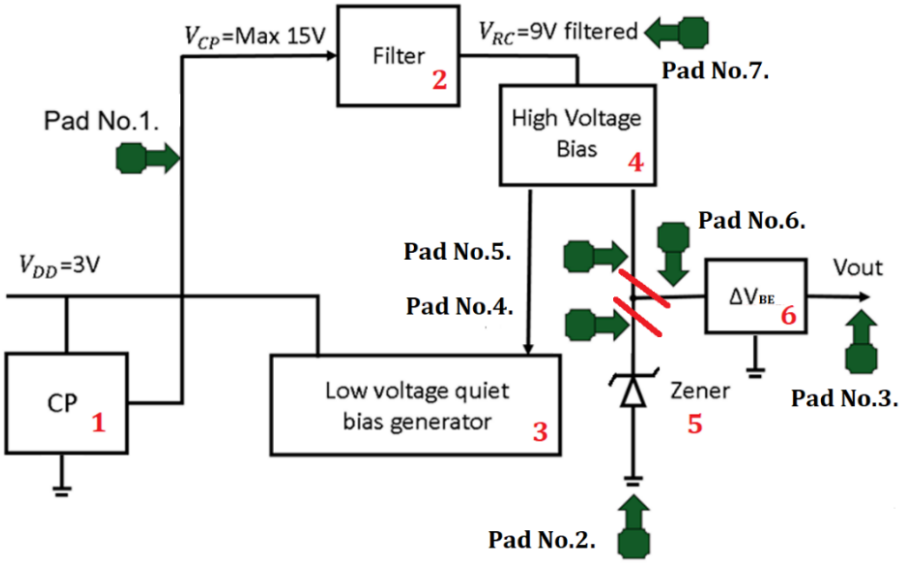

Figure 4.12 Zener-TC2 block diagram of available pins enabling design modularity and future developments

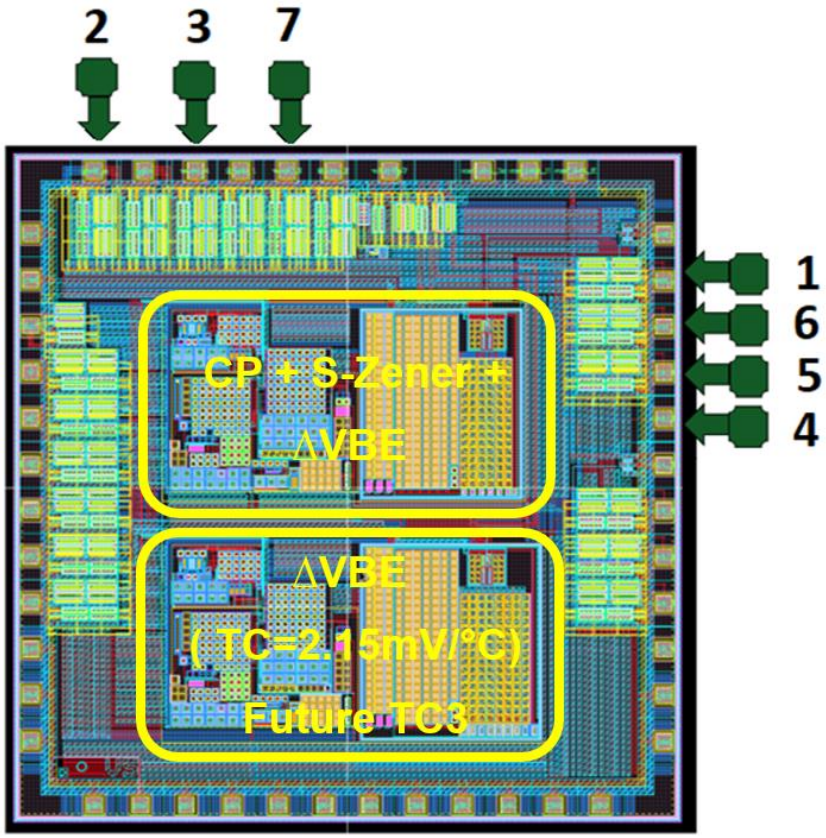

Figure 4.13 Zener-TC2 layout view of available pins enabling design modularity and TC3 ΔV_{BE} future correction

This modular approach was critical to the fast development of the future prototypes with little financial implications and very fast return times.

Chapter 5

TC3 High Performance B-Zener

5.1 TC3 high performance B-Zener based architecture

As stated previously in Chapter 2, having available all the necessary components on the 0.6μm Bi-CMOS ADI proprietary process including the S-Zener diode, the process was

the obvious choice for the physical implementation of our **TC1** & **TC2** test chips. Based on detailed analysis in Chapter 2, it become obvious that the Zener diode native to the selected 0.6μm Bi-CMOS process was the less accurate surface Zener type and not the high-performance buried Zener one. The S-Zener used in **TC1** and **TC2** has been identified as the main error source and a limitation factor in our design. Replacing the **S-Zener** with a high-performance **B-Zener** and co-package the two ICs is the obvious choice here. Based on our extensive investigation in Chapter 2, including both the **S-Zener** and **B-Zener** uncompensated diode variants, the optimal **PTAT** biasing current was identified resulting in an induced minimum nonlinearity in the output reference voltage. Selecting any other operation bias current will introduce by default a non-optimal larger than minimum nonlinearity component. This degree of freedom will require further investigation to enable us a state of art noise performance in our design. User selectable bias currents for low **25uA** to high **500uA** in **25uA** increments are available, to analyse in-package bias magnitude nonlinearity influence to confirm our developed model. The active region of the new B-Zener diode is significantly larger when compared to the embedded one from **Zener_TC1**. This area increase should provide an improvement in noise reduction in line with the theoretical values [19]. For applications where the overall noise is the key specification, the only possible solution is to select an appropriate biasing current of the required magnitude. This non-optimal biasing current will introduce a larger than minimum nonlinearity in our output voltage as per **Chapter 2**. Having available both the mathematical model and the novel compensation technique presented in **Chapter 6**, one can decouple the bias requirements from the overall **TC** requirements by adjusting the nonlinearity overall components to suit our design key specifications [20].

5.2 TC3 IC packaged evaluation measurements

Having at our disposal all the building blocks needed already manufactured and available from **Zener_TC2** test chip, implementing the novel **Zener_TC3** was relatively straight-forward and was finalised without any technical difficulties. Co-packaging the two-silicon dies together (the Buried Zener diode and the ΔV_{BE} plus the trimming circuits) in a plastic package (Shrink Small Outline **150mil body QSOP** as per Figure 5.1.) was finalised with a very short turnaround time.

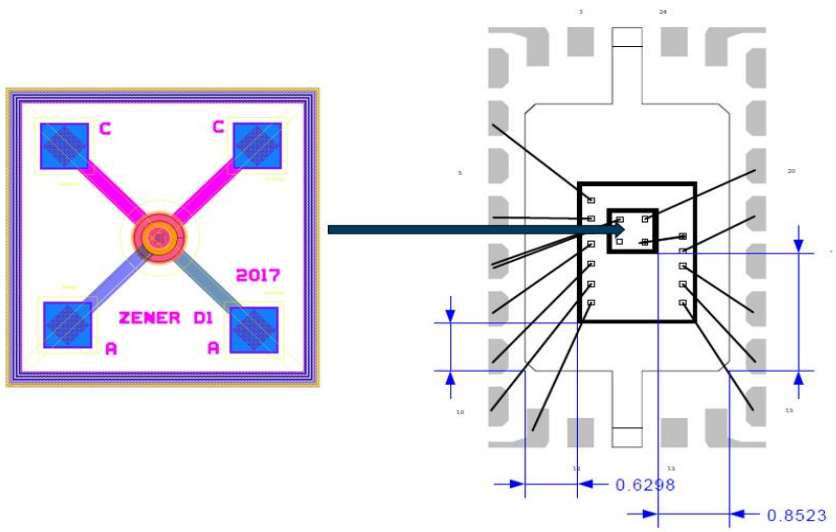

Figure 5.1 Zener-TC3 co-packaged die details for 150mil body QSOP

Measurements for **Zener_TC3** compensated $Vref$ were performed at **25 °C** for **100** random samples post individual optimal trim. A histogram associated with these **100** random device measurements is presented in Figure 5.3. Based on these measurements a standard deviation at **25°C** of **4.2mV** and a mean value of **6.14V** was calculated for all 100 measured ICs. Based on these 100 samples an initial accuracy of **<0.5%,** for six sigma distribution was calculated.

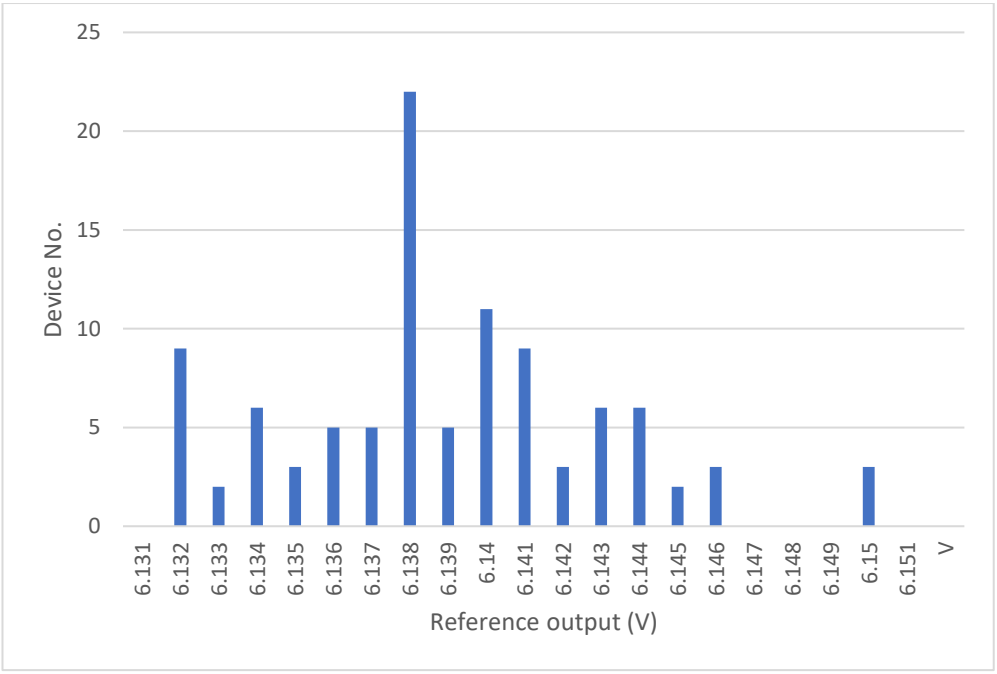

Figure 5.3 Measured Zener-TC3 standard deviation at 25°C of 4.18mV and a mean value of 6.141V

Measurements for **Zener_TC3 TC** were performed from **-40°C to 125°C** without gain calibration, but with individual optimal trim codes. The plot of the compensated Zener-based reference voltage output vs. temperature, based on a sample of **50 QSOP** IC packaged die measured in oil bath is presented in Figure 5.4.

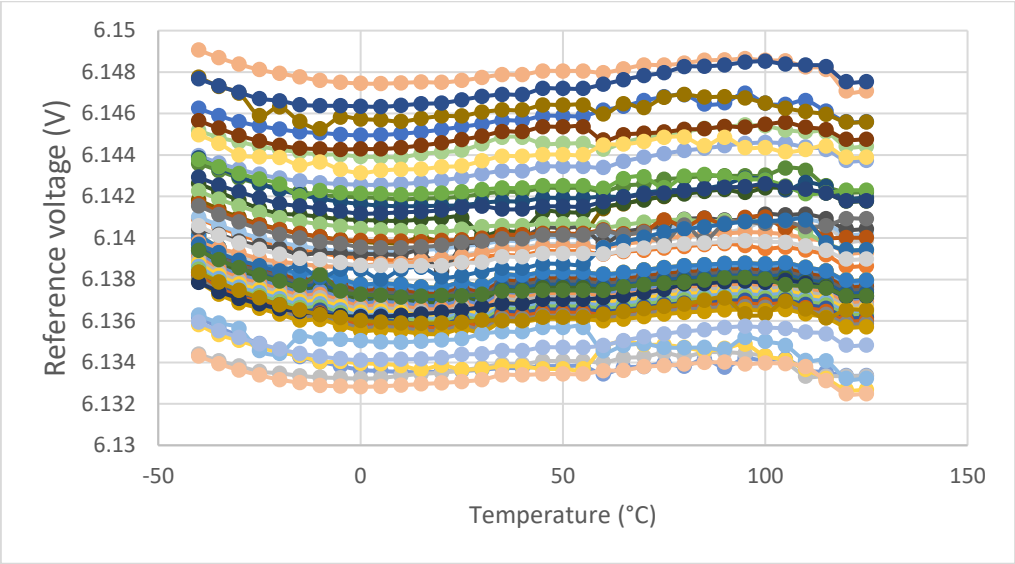

Figure 5.4 Measured Zener-TC3 reference voltage temp. dependency for full industial range (-40°C to 125°C)

Based on these measurements, the nonlinearity associated with the new proposed B-Zener based architecture was calculated. These values are presented in Figure 5.5.

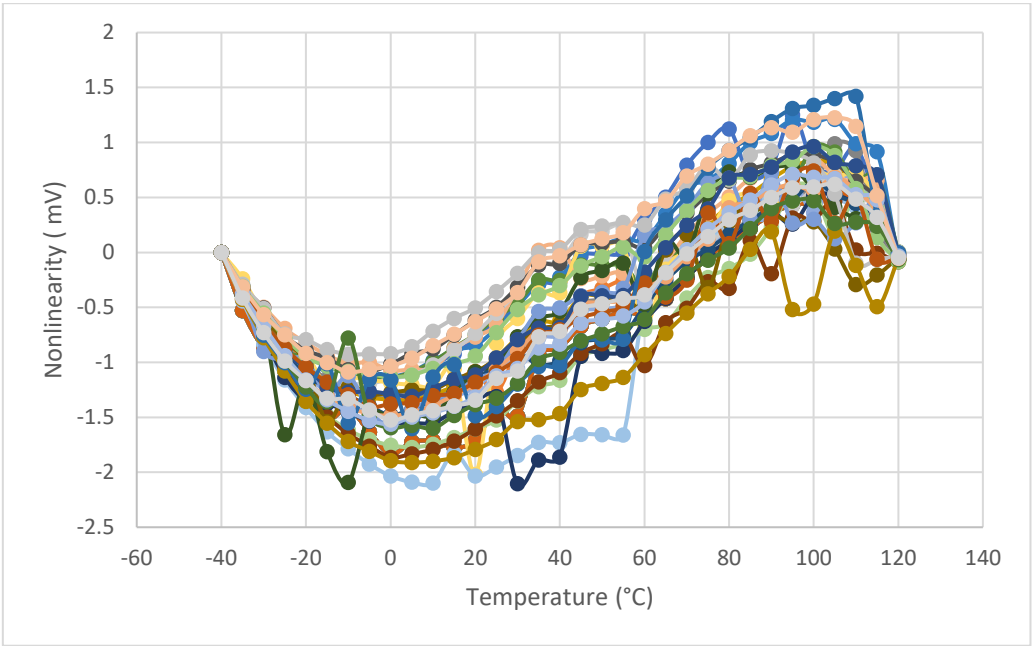

Figure 5.5 Zener-TC3 B-Zener measured nonlinearity vs. temperature

Using the industry standard box method for the calculation of temperature coefficients (**TC**), a **min-max TC of 1.34 – 3.99ppm/°C** was calculated for all **50 QSOP** measured parts. The TC histogram associated with these measurements is presented in Figure 5.7.

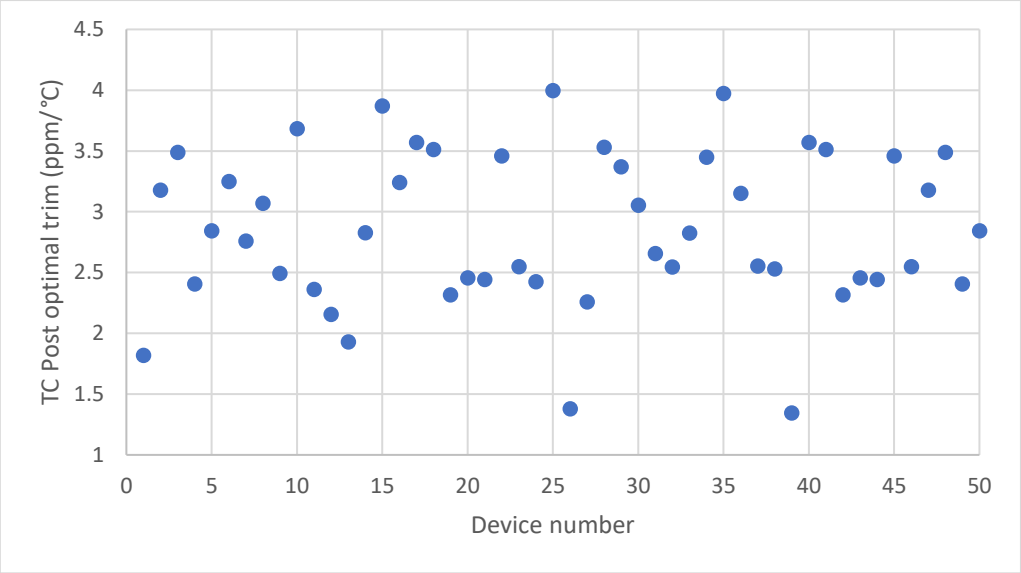

Figure 5.7 Zener-TC3 TC values (based on 50 random samples) for industrial temperature range

Initial Re-Flow silicon measurements were performed on **30 QSOP** plastic packaged ICs **Zener_TC3** architecture chips. Based on these measurements a **Mean** = **170uV,** and a standard deviation of **σ=88uV** was calculated. The **SHR Min-Max** values measures were **(50uV- 330uV)** with a range of **280uV**. The drift histogram associated is presented in Figure 5.9. A reduced drift was observed vs. Zener_TC1 due to the innovative high-performance B-Zener diode utilised in Zener_TC3 IC test-chip.

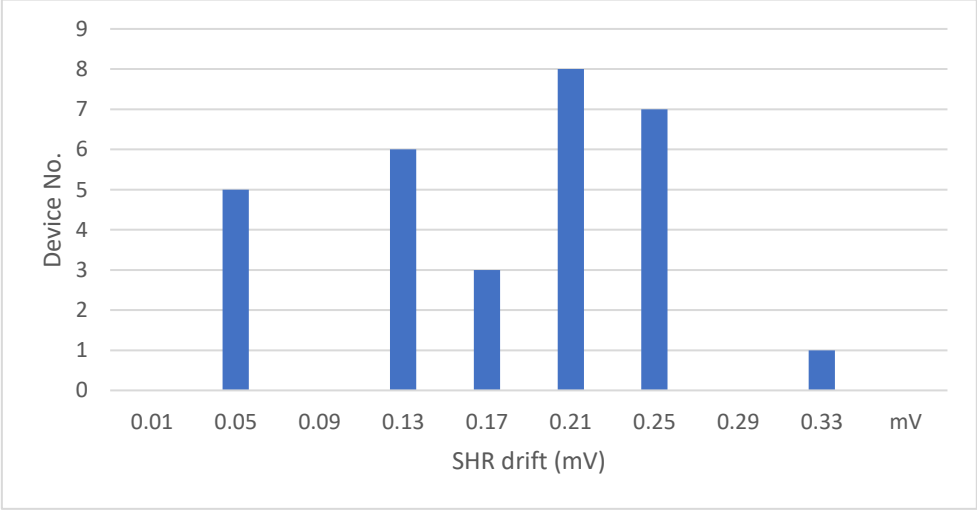

Figure 5.9 Zener-TC3 measured B-Zener compensated Re-Flow drift

This measured drift represents a reduction of more than +**75%** when compared with the initial embedded **Zener_TC1** proposed architecture design [6].

Chapter 6

Base-emitter voltage linearization

6.2 Correction circuit basic implementation

A circuit according to the theory from **Chapter 6.1**, based on [16], [9], can reduce both base-emitter voltage spread and its nonlinearity had been developed as presented in Figure 6.5.

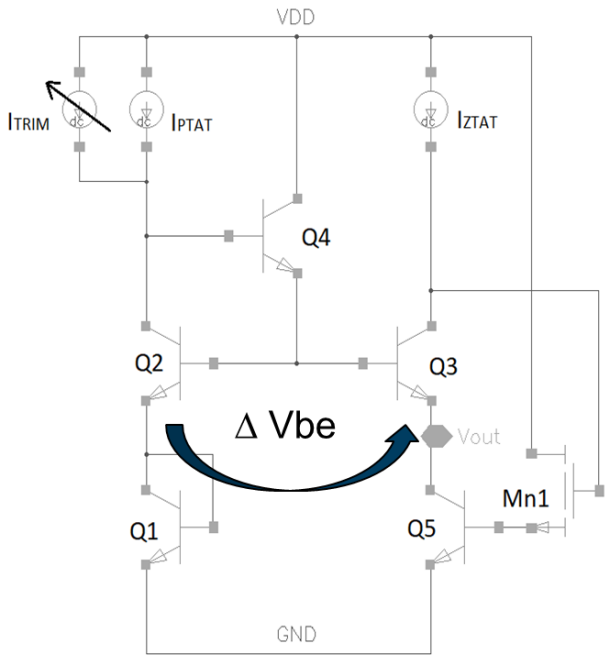

Figure 6.5 Novel proposed circuit compensation basic principle

The circuit in Figure 6.5. is based on a diode connected BJT, **Q1**, and a pair of BJTs with common base, biased differently, **Q2** with **PTAT** current and **Q3** with **ZTAT** current. The role of $\boldsymbol{Q4}$ (known as beta helper) [21], [9], is to supply the base currents of $\boldsymbol{Q2}$ and $\boldsymbol{Q3}$. The MOS transistor MN1 and bipolar transistors **Q3**, **Q5** act together as

an amplifier producing at the output node a voltage matching the $\mathbf{V_{BE}}$ of **Q1** plus the base-emitter voltage difference from **Q3** to **Q2**. As a result, the output voltage is:

$$V_{out} = V_{BEQ1} + V_{BEQ2} - V_{BEQ3} \tag{6.14}$$

The output voltage nonlinearity is expressed by:

$$V_{out-nonlin} = -\frac{kT}{q}(XTI - 1)\ln\frac{T}{T_0} + \frac{kT}{q}\ln\frac{T}{T_0} = -\frac{kT}{q}(XTI - 2)\ln\frac{T}{T_0} \tag{6.15}$$

Usually, XTI factor is of the order of 3 to 4 [22] and as such that the output voltage nonlinearity must be reduced further. If this cell is followed by a similar ΔVbe cell (with no diode connected device, Q1) in which a first transistor will be biased with **PTAT** current and a second transistor biased with **ZTAT** current, the novel output voltage nonlinearity is reduced more. The NMOS device NM1 and BJT Q5 have several functionalities. First, at the emitter of transistor Q3 they generate the voltage difference $V_{BEQ2} - V_{BEQ3}$ directly dependent to the collector current density of the two bipolar transistors. Second, they limit the V_{CBQ3} swing and in such reducing the Early drift. The (W/L) aspect ratio of NMOS MN1 will be chosen as such that the V_{CBQ2} and V_{CBQ3} track each other to minimize the overall Early related drifts. Finally, with a stack of three or four ΔV_{BE} cells (depending on the Q2 to Q3 collector current density ratios) the output voltage nonlinearity is reduced close to zero. This nonlinearity can be then corrected as needed by adjusting the **ZTAT** current accordingly, little more **PTAT** or little more **CTAT**. The base-emitter voltage spread can then be compensated the by **PTAT** DAC converter **ITRIM1** as shown in Figure 6.5.

The non-linear term of a ΔV_{BE} voltage whose **LCD** device is biased with a **ZTAT** current has an opposite sign to that of a V_{BE} voltage, and a magnitude of one thermal voltage as presented in earlier.

$$V_{out} = V_{BEQ1} + V_{BEQ2} - V_{BEQ3} \tag{6.16}$$

The proposed circuit will reduce the temperature dependency of $V_{BE}(T)$ in twofold:

1. Reducing the spread of the $V_{BE}(T)$ by means of trimming the bias current of the diode connected device Q1, as per Figure 6.5.
2. Reducing the nonlinearity of the $V_{BE}(T)$ by means of a novel compensation circuit (named ΔV_{BE}).

6.3 High performance temperature sensor design

A complete standalone design in accordance with the principles described in Figure 6.5 was designed, simulated, and is ready to be manufactured. Identical BJT devices areas are used for the BJTs with a common base (Q2, Q3 and so on). **PTAT** and **ZTAT** bias currents are used to force those collector currents in two matched BJTs. As each ΔV_{BE} cell provides approximately 1mV of voltage nonlinearity reduction and typically BJT V_{BE} nonlinearity is approx. **4mV**, four ΔV_{BE} cells are required to reduce the overall nonlinearity to close to zero, as Figure 6.8 shows. The overall simulated nonlinearity is reduced to max ±**600nV**.

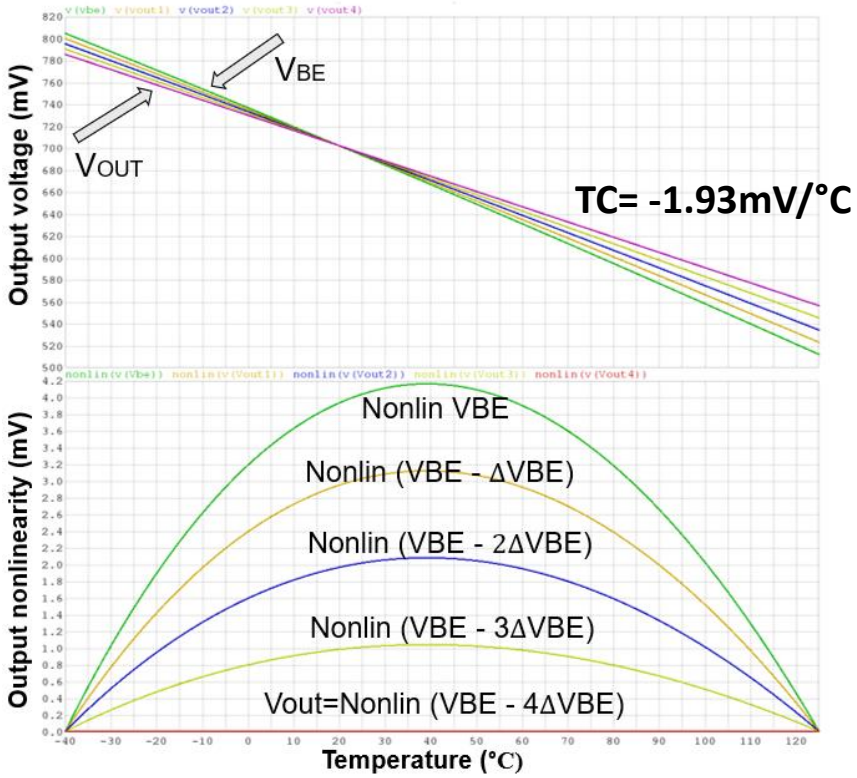

Figure 6.8 V_{BE} nonlinearity component, compensated by four ΔV_{BE} cells

6.6 Compensation technique advantages

This design investigates an innovative method of correcting a V_{BE} BJT temperature dependency by reducing both the base-emitter voltage spread and its nonlinearity temperature variation using an innovative ΔV_{BE} cell design. With its reduced temperature dependent nonlinearity and good sensitivity, the circuit meets the criteria for a high-performance temperature sensor.

The main advantages of the new proposed circuit are:

- High temperature sensitivity of **-1.93mV/°C.**
- Overall sensor accuracy **better than 0.2°C for -40°C to 125°C** temperature range.
- Overall sensor accuracy **better than 0.168°C for 0°C to 85°C** temperature range.
- Resistor-less architecture for the core cell.
- Low output impedance [16], [9].
- Simple and effective trim method to compensate the Spread of $V_{BE.}$
- Simple and effective trim method to compensate nonlinearity by use of ΔV_{BE} cells.
- As the area report of the BJT is 1:1 there is no need for leakage compensation.
- Lower noise compared to [16], [9] due to the reduction in ΔV_{BE} cells (4 vs. 6).
- Small silicon area ~ $\boldsymbol{1.5\ sqmm}$ for the complete test chip.
- Single point trim will provide adequate precision to meet the required nonlinearity performance criteria.

Chapter 7

Conclusions

The objective of this thesis is to improve the power-related FoM of the most stable, "State of the Art" silicon-based voltage reference, based on Zener diodes. This research has covered both aspects of the Zener diodes temperature dependency: measurement-based theoretical models and the practical perspectives, in terms of architecture and circuit design combined with physical implementation, full manufacturing flow and plastic packaged IC evaluation. Following established compensation architectures (Stefan Marinca **US9323275B2** [23]), adapted and enhanced to our specific circuit needs, a cost effective, package independent, **non-heated** silicon-based voltage reference with a **TC** in low single digits ppm figures over the full temperature industrial range (**−55°*C* to 125°*C*)** was developed. A post manufacturing IC packaged die, simple, flexible & effective trimming circuit was also developed for both the linear and nonlinear components, and as a result making possible to achieve the low TC imposed in the research objectives.

Investigating and mitigating all other thermal IC packaged related influences like **SHR**, **LTD** and **Hysteresis**, which are directly impacting the final temperature IC performance, were particularly important to this thesis. Reducing the package induced stress of the novel developed plastic ICs first, by the inherited resilience of the B-Zener diode and second by the novel ratio metric ΔV_{BE} cell developed (less susceptible to mechanic/electrical stress), opens original new avenues for further research into the elusive 1ppm/°C temperature coefficient drift for a non-heated silicon-based voltage reference.

In conjunction with circuit research, an original measurement-based temperature dependency numerical model for a B-Zener diodes has been developed in this thesis. This model has resulted in an optimal correlation between simulation and silicon results. Motivated by the need to compensate the nonlinear term of the thermally uncompensated Zener diode native temperature variation, a new USA Patent (**Application APD6917US01 January 2020** and **WOS: 000538328000046**), was filed based on this innovative compensation principle. This novel compensation architecture was proven by utilising an advanced prototyping solution, with spectacular linearization improvements (orders of magnitude) when compared with the initial input values. Similar nonlinearity correction techniques could be applied to the uncompensated **B-Zener** diode output voltage incorporated in the ΔV_{BE} cell itself. The thesis has presented both the means and the compensation method for the 1st and 2nd order terms, associated with a Zener diode temperature dependency. A high-performance family of **Non-Heated Zener-based** voltage references was successfully developed in this thesis.

7.1 Original contributions and discussion of results

All the material presented in Chapter 2, Chapter 3, Chapter 4, Chapter 5 and Chapter 6 represents the original work of the author, under guidance from Prof. Dr. Mircea Bodea and Prof. Dr. Stefan Marinca. This work includes the development of the architecture of each cell variant, the detailed circuit design and physical implementation, as well as the interpretation of the measured silicon results. The original contribution of others was fully referenced and acknowledged appropriately.

The original contribution of the author presented in this thesis can be summarised as follows, in chronological order:

(OC1) A measurement-based temperature dependency numerical model for both **S-Zener** and the **B-Zener** (based on non-heated silicon configuration) diodes was developed initially. This allows us to select an optimal Zener bias current with a direct implication for minimal bias induced nonlinearity, while also improving the correlation between the simulation and silicon results.

(OC2) Based on **(OC1)**, a novel compensation principle was developed for a non-heated silicon substrate Zener diode. This novel embodiment was developed as a spinoff of an existing circuit architecture (Stefan Marinca **US9323275B2** [23]). A full ICs circuit consistent with the above principle was designed, SPICE simulated and physically implemented in a standard manufacturing process 0.6um Bi-CMOS. Several fully assembled (**30 die) PLCC** plastic packaged **TC1** ICs were submitted to a full prototype evaluation cycle. The highlights of the **TC1** measured performance are low **TC** for all the measured ICs varying between **1ppm/°C <TC< 6.5ppm/°C** (for all the 30 parts, over the full industrial temperature range of **−55°C to 125°C**)**,** easy and effective temperature coefficient **(TC) trimming,** and small silicon footprint **(~1sqmm)**. Good immunity to package induced stress was measured at only **SHR < 400ppm,** due to the ratio-metric nature of the ΔV_{BE} compensation circuit. Based on this research developed in (OC2), a paper entitled "*Low Drift Zener-Based Voltage Reference"* was submitted for peer review and positive feedback was received at the 26th Irish Signals and Systems Conference (ISSC), Ireland, 2015, **WOS: 000380490400034.**

(OC3) An enhancement to the (**OC2)** was developed subsequently. This novel architecture, named **TC2**, benefits from a reduced supply requirement of **Minimum=2.7V**, in the normal operating mode, while maintaining all other specifications of **TC1** unaffected. A Charge Pump front end was implemented to reduce supply requirements, while advanced design techniques were applied to reduce the CP noise coupling to the output reference. Another highlight of the **TC2** die is the **"Lego Like"** modular approach that enables us to perform an individual evaluation of the output components contributions in the overall reference value. A full ICs circuit consistent with the above principle was

designed, SPICE simulated and physically implemented in a standard manufacturing process. Several (**50 die)** assembled **TC2 LFCSP** plastic packaged ICs were submitted to a full prototype evaluation cycle. Based on these, the **S-Zener** diode itself was identified as a major limiting factor of the overall IC performance. Based on this novel architecture enhancement developed in (**OC3),** a paper entitled "*An Embedded Charge Pump for a Zener-Based. Voltage Reference Compensated Using a Delta VBE Stack",* was presented with very positive feedback at the *24th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES),Poland, 2017.* The paper received an **"Outstanding Paper Award"** acknowledgement at the above Conference, **WOS: 000426980600039.**

(OC4) An enhancement to the **TC2** original architecture solution (presented in (OC3)) was developed subsequently. Mitigating the **S-Zener** limited performance, a novel architecture **TC3,** including a high-performance **B-Zener** diode was proposed. Several (**100 QSOP packaged ICs)** co-packaged B-Zener and associated compensation circuits were submitted to a full prototype evaluation cycle. The highlights of **TC3** performances include a reduction in **TC** variation of **1ppm/°C <TC< 4ppm/°C** (over the **−55°C to 125°C** temperature range) and a **Re-Flow** drift of **SHR < 50ppm (**equivalent of an **+75%** improvement**)** when compared to the original **TC1 ICs.** Based on this novel compensation concept developed in this thesis, a paper entitled "*A Zener-Based Voltage Reference Design Compensated Using a Delta V_{BE} Stack"* was presented at the "25th International Conference on Mixed Design of Integrated Circuits and System (MIXDES), Poland 2018. The paper received an **"Outstanding Paper Award"** recognition at the above Conference, **WOS: 000480458200018.**

(OC5) An analog high-performance temperature sensor was developed subsequently. Based on a novel compensation concept (patent pending), an innovative V_{BE} nonlinearity correction method was proposed. This novel proposed architecture is at advanced prototyping stage, having completed a full detailed circuit design, SPICE simulation, device analysis, layout implications and is awaiting manufacturing. The temperature sensor performances for the novel circuit simulated at device level, post parasitic extraction are a high

sensitivity of **ΔV/ΔT=--1.93mV/°C** and a nonlinearity error of maximum **0.04°C** for the **-40°C to 125°C.** When reducing the temperature range to **0°C to 85°C**, this nonlinearity corresponds to a maximum error measured of **0.008°C**. Based on this novel compensation concept developed a paper entitled "*Reducing the Bipolar Junction Transistor V_{BE} Non-Linearity",* was presented *at the* 26th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), Poland 2019. The paper received an **"Outstanding Paper Award"** acknowledgement at the above Conference, **WOS: 000538328000046.**

(OC6) Based on **(OC5),** a novel correction method was incorporated into **(OC4)**. The linear (flip ΔV_{BE}) compensation circuit proposed in (**OC2)** can be enhanced to facilitate the Zener-based reference design nonlinearity term correction in the same manner as in (OC5). This new circuit (named **TC4**) implementation will allow decoupling the Zener bias value term (and in such the baseline noise value for the Zener diode) from the output reference nonlinearity. This novel TC4 architecture is the subject of further research.

A table of performance comparations between the developed architectures (detailed in Table I), are presented below in Table VI.

TABLE V. ZENER_TC1, TC2, TC3 AND TC4 KEY PERFORMANCES

Part ID	Zener_TC1	Zener_TC2	Zener_TC3	Zener_TC4
Vdd Supply (V)	6.5	3	7.5	7.5
Vout (V)	4.8	4.8	6.15	6.15
I quiescent(mA)	0.1	0.4	0.15	5.1
TC (ppm/°C)	1 to 6.5	1 to 6.5	1 to 4	<2
Initial accuracy	1%	1%	0.50%	0.50%
SHR (ppm)	~400	~400	<50	<50
Noise uVp-p 0.1-10Hz	30	50	~10	~1
FoM (Noise*Idd*Vdd) $(mVW)^{-1}$	**51**	**16**	**88**	**26**
Reference Principle	S-Zener + ΔV_{BE}	CP+S-Zener + ΔV_{BE}	B-Zener + ΔV_{BE}	B- Zener + ΔV_{BE} +nonlin adj.

When comparing these performances versus the established architectures (both TCUBZ and BGA presented in Table I), we can identify strengths of the proposed architecture that can provide the best of both worlds solutions: low power supply requirements (specific to the bandgap voltage type references) and extremely low TC, LTD and SHR (specific to the buried Zener type references). An extract from the Table I, with best-in-class specific architecture performance comparations are presented in Table VII.

TABLE VI. ESTABLISHED ARCHITECTURES PERFORMANCES

Reference Principle	**BGA**	**TCUBZ**	**TUCBZ**
State of the Art	**ADR45XX**	**LTZ1000**	**TC1 - TC4**
Initial Accuracy	±0.02%	4%	1% - 0.5%
TC ppm/ºC	~4	<1	1 to 4
SHR ppm	100+	High	<40
Long term drift (LTD)	+50ppm/1Kh.	~2 ppm/1Kh	Low ppm/1Kh
Output noise (0.1–10 Hz) uVp-p	2	1	1
FoM (Noise*Idd*Vdd)(mVW)$^{-1}$	**166**	**0.952**	**16 to 88**
Input voltage (V)	3 to 15	Min 10	3 to 15
Output voltage (V)	2.048 to 5	Min 7	4.8 /6.15
Quiescent current:	1mA+ (Ref+Buffer)	5mA (Zener only) 300mA Heater	0.1 to 5.1mA + (No Buffer)
External components	None	Full PCB build	None
Operating temperature	-40ºC to +125ºC	-55ºC to +125ºC	-40ºC to +125 ºC
IC Package	MSOP 8	TO-5 Metal	Plastic
Cost per unit	2.45 USD	~50 USD	Low USD

As highlighted in Table VI, the self-created **FoM** based on (Noise*Power Supply *Current consumption) factors, has placed the **TC1 - TC4** ICs in proximity of the acclaimed ADR**45XX** of Analog Devices based on Stefan Marinca architecture [24], but having better **TC**, **SHR** and **LTD** parameters and orders of magnitude ahead of heated-substrate **LTZ1000** due to high energy requirements of the second one, while maintaining comparable noise and temperature dependant performances.

7.2 List of original works

(OW1) **"Best Paper Award"**, Dragos Dobrescu, Viorel Bucur, Lidia Dobrescu "8 Bit Pre-Setable Digital to Analog Converter Design" ICSTCC: Proceedings of the 22-nd International Semiconductor Conference, CAS'99, Sinaia, Romania, vol.1, pg. 73-76, INDEX IEEE.

(OW2) Viorel Bucur "Bandgap based 10 Bit DAC IC with Slope & Offset Correction Capabilities" Master of Engineering, VLSI Systems – Year 2006, University of Limerick.

(OW3) Marinca, S and **Bucur, V,** *Low Drift Zener-Based Voltage Reference,* Conference: 2015 26th Irish Signals and Systems Conference (ISSC) , Web of Science Categories: Computer Science, Artificial Intelligence; Computer Science, Interdisciplinary Applications; Engineering, Electrical & Electronic, Accession Number: **WOS: 000380490400034**, ISBN: 978-1-4673-6974-9, Publisher: IEEE.

(OW4) **"Outstanding Paper Award", Bucur, V**; Banarie, G; Bodea, M, *An Embedded Charge Pump for a Zener-Based. Voltage Reference Compensated Using a Delta V-BE Stack,* Conference: 2017 24th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), pp.215-219, Web of Science Categories: Computer Science, Artificial Intelligence; Computer Science, Interdisciplinary Applications; Engineering, Electrical & Electronic, Accession Number: **WOS: 000426980600039**, ISBN:978-8-3635-7812-1.

(OW5) Marinca, S; Banarie, G; **Bucur, V,** Bodea, M, *A +/- 2m degrees C Linearity Silicon Temperature Sensor,* Conference:2017 International Symposium on Signals, Circuits and Systems (ISSCS), Web of Science Categories: Computer Science, Artificial Intelligence; Computer Science, Interdisciplinary Applications; Engineering, Electrical & Electronic, Accession Number:

WOS: 000425211500086, ISBN: 978-1-5386-0674-2, Publisher: IEEE.

(OW6) **"Outstanding Paper Award", Bucur, V**; Banarie, G; Bodea, M, *A Zener-Based Voltage Reference Design Compensated Using a Delta V-BE Stack,* Conference: 2018 25th International Conference on Mixed Design of Integrated Circuits and System (MIXDES), pp.116-120, Web of Science Categories: Computer Science, Artificial Intelligence; Computer Science,

Interdisciplinary Applications; Engineering, Electrical & Electronic, Accession Number: **WOS: 000480458200018**, ISBN**:** 978-8-3635-7814-5, Publisher: IEEE.

(OW7) Banarie, G; McDonagh, D; **V, Bucur**; Bodea, M, *A BJT Bi-CMOS Temperature Sensor with a Two-Point Calibrated Inaccuracy of 0.1 degrees C (3 sigma) from-40 to 125 degrees C*, Conference 2018: 29th Irish Signals and Systems Conference (ISSC), Web of Science Categories: Computer Science, Artificial Intelligence; Computer Science, Interdisciplinary Applications; Engineering, Electrical & Electronic, Accession Number: **WOS: 000462519500022**, ISBN:978-1-5386-6046-1, Publisher: IEEE.

(OW8) **"Outstanding Paper Award", Bucur, V**; Banarie, G; Bodea, M, *Reducing the Bipolar Junction Transistor V_{BE} Non-Linearity,* Conference 2019*:* 26th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), pp.256-259, Web of Science Categories: Computer Science, Artificial Intelligence; Computer Science, Interdisciplinary Applications; Engineering, Electrical & Electronic, Accession Number: **WOS: 000538328000046**, ISBN: 978-83-63578-16-92, Publisher: IEEE.

(OW9) Viorel Bucur Patent Application APD6917US01 "A Circuit for Generating a Temperature Dependent Output" Filed January 2020.

7.3 Future research

The venerable Bipolar Transistor is over 74 years old, [25]. After all this time of research and development, the Art of Pure Analog Circuit Design continues to discover innovative areas for improvement by better understanding the principles and inventing novel ways of mitigating shortcomings in the device itself [26]. With the latest developments in silicon manufacturing, signal processing and digital computation, there is less need for a "Pure" analog only circuit approach, but there will always be a demand for ultra-high performance voltage references and temperature measuring architectures implemented in the analog only domain.

An in-depth analysis into the Zener Device Solid State Physics should be performed to determine if the selected temperature dependency numerical model from Chapter 2, based on the industry standard SPICE models analysed was the optimal one. After determining the optimal mathematical approximation based on the Zener Device Solid

Physics temperature dependency, a larger sample of fully plastic packaged ICs should undergo a full prototype evaluation cycle. Based on this new large sample data corroborated with a novel numerical model, a higher degree of confidence will be attained and a product "**Data Sheet**" available for customer reference can be created. All the known necessary precautions were taken during both the design stage and the physical implementation stage. Sufficient safety margins were incorporated in all the aspects of the chip design to maximise our chances to meet the design targets.

A novel circuit (**Zener_TC4**) based on the already designed **Zener_TC3,** should be subjected to a full prototype evaluation cycle. The "**Key specifications** "for the novel **Zener_TC4** will be that of max noise performance combined with an ultra-low-TC. As presented in **Chapter 2,** the B-Zener bias diode alone will require **~5mA** of bias to obtain comparable noise values as **LTZ1000/ADR1000** [3], [4]. All the necessary numerical models, architectures, circuit design and silicon building blocks required are available now to design and manufacture a truly state of the art B-Zener based non-heated reference voltage device.

For a further reduction in package induced stress, a 3 pyramidal structure of die co-package SIP solution can be implemented, providing maximum immunity to the Package Induced Stress of any nature, as described in [27].

This 3-tier pyramidal combination could be arranged as follows for optimal mechanical reducing stress:

- **Die 1**
  - **Buried Zener -** Stress immunity, stability, and a mechanical buffer for Package Induced Stress to the **Die 2** and **Die 3.**
- D**ie 2**:
  - **Charge Pump** - Noise immunity, CP efficiency and a buffer for Package Induced Stress to the Flip ΔV_{BE} block.
- **Die 3**
  - **Flip ΔV_{BE} cell** - Maximum mechanical protection containing the ΔV_{BE} correction circuit and all other critical **CMOS** blocks.

This pyramidal structure will allow us to maximise each of the 3-block component's strengths while the other blocks are also acting as a package stress buffer, protecting the most critical and stress-prone block (the Flip ΔV_{BE} circuit, as described in Chapter 3).

Selective References

[1] G. C. M. M. a. A. B. F. Fruett, “Minimization of the mechanical-stress-induced inaccuracy in bandgap voltage references,” *IEEE Journal of Solid-State Circuits,* vol. 38, no. 7, pp. 1288-1291, 2003.

[2] W. G. Eicke, “Commentaires sur l’utilisation des diodes de zener comme etalons de tension,” *Comite´ Consultatif d’E´lectricite´,* no. 11e Session, pp. 1874-1877, 1963.

[3] A. Devices, “LTZ1000 Data Sheet,” Analog Devices, https://www.analog.com/en/products/ltz1000.html#product-overview, 2021. [Online]. Available: https://www.analog.com/en/products/ltz1000.html#product-overview.

[4] R. Kaußler, “Richi's Lab Semiconductor ADI1000,” Richard Kaußler, Schernfeld, https://www.richis-lab.de/REF19.htm, 2019.

[5] G. B. S. M. M. B. Viorel Bucur, “An Embedded Charge Pump for a Zener-Based Voltage Reference Compensated Using a ΔVBE Stack,” in *MIXDES*, 2017.

[6] V. B. Marinca Stefan, “Low Drift Zener-Based Voltage Reference,” *Signals and Systems Conference (ISSC), 26th Irish,* 2015, WOS:000380490400034.

[7] ROHM, “ROHM Spice Model Database,” Japan, 2015, https://www.pspice.com/models/rohm.

[8] R. Semiconductor, “Zener PSpice Rohm model,” ROHM Semiconductor, HK, 2015, https://fscdn.rohm.com/en/products/library/spice/discrete/diode/zener/cdz4_7b.zip.

[9] V. Bucur, “Reducing the Bipolar Junction Transistor VBE non-linearity,” in *Mixed design of Integrated Circuits and Systems*, Poland, 2019, WOS:000480458200018.

[10] K. W. M. David Johns, in *Analog integrated circuit design*, John Wiley & Sons, 1997, ISBN: 0-471-14448-7, p. 353.

[11] S. Marinca, “Ultralow Noise, High Accuracy Voltage Reference, Analog Devices, Inc. datasheet ADR45XX,” Analog Devices, 2012.

[12] E. L. (LE), “For series production suitable circuits of temperature-stable low-voltage power supply cards,” KFK-218, KITopen ID: 270000958, DOI: 10.5445 / IR / 270000958, 1964.

[13] D. A. J. K. W. M. Tony Chan Carusone, “ Analog Integrated Circuit Design 2nd Edition,” Wiley Global Education, 2011, pp. 310-311.

[14] D. A. J. K. W. M. Tony Chan Carusone, “Analog Integrated Circuit Design" 2nd Edition,” Wiley Global Education, 2011, ISBN-10: 0470770104, p. 319.

[15] S. Marinca, “Low drift voltage reference”. USA Patent APD5029 , 1 11 2013.

[16] S. Marinca, “Method and circuit for low power voltage reference and bias current generator”. USA Patent US8531169B2.

[17] T. Instruments, “Dateseet: REF102 Zener based 10-V Precision Voltage Reference,” https://www.ti.com/lit/ds/symlink/ref102.pdf?ts=1645044376116&ref_url=https%253A%252F%252Fwww.google.com%252F, 2022,.

[18] D. Clein, “CMOS IC Layout: Concepts,” in *Methodologies, and Tools*, Newnes, Newnes, 1999, ISBN - 978-0750671941, pp. 155-158, 170-172.

[19] D. M. Binkley, “Tradeoffs and Optimization in Analog CMOS Design,” John Wiley & Sons, Ltd , 2008, pp. 440-441.

[20] K. Enslein, “Characteristics of silicon junction diodes as precision voltage reference devices,” *IRE TRANS. ON INSTRUMENTATION, aging to prove stability,* vol. 1, no. 6, pp. 105-118, 1957.

[21] R. J. Widlar, “New developments in IC voltage regulators,” *IEEE Journal of Solid-State Circuits,* Vols. vol. SC-6, no. 1, pp. 2-7, 1971.

[22] Y. P. Tsividis, “Accurate analysis of temperature effects in IC VBE characteristics with application to bandgap reference sources,” *IEEE J. Solid-State Circuit,* no. SC-15, pp. 1076-1084, 1980.

[23] S. Marina, “Proportional to absolute temperature circuit”. USA Patent US9323275B2, 11 12 2013.

[24] S. Marinca, “Method and circuit for low power voltage reference and bias current generator”. USA Patent US9218015B2, 09 July 2012 .

[25] W. Shockley, “The Theory of P-N Junctions in Semiconductors and P-N Junction Transistors,” *Bell System Technical Journal,* vol. 28, no. 3, pp. 435-89., July 1949.

[26] G. B. S. M. a. M. B. V. Bucur, “A Zener-Based Voltage Reference Design Compensated Using a ΔVBE Stack,” in *25th International Conference "Mixed Design of Integrated Circuits and System" (MIXDES), 2018, pp. 116-120,* 2018, WOS: 000480458200018.

[27] E. G. F. Vasilis F. Pavlidis, “Manufacturing of 3-D Packaged Systems,” *Three-dimensional Integrated Circuit Design,* 2009.