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Ph.D. THESIS SUMMARY

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POTENŢIOMETRE DIGITALE CU PERFORMANŢE ÎMBUNĂTĂŢITE CU APLICAŢII ÎN SISTEMELE AUDIO-VIDEO

DIGITAL POTENTIOMETERS WITH IMPROVED PERFORMANCES WITH APPLICATIONS IN AUDIO-VIDEO SYSTEMS

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Chapter 1

Introduction

1.1 Presentation of the field of the doctoral thesis

In the last period the demand for complex and performant integrated systems has incredibly increased in the electronic industry. This kind of systems should consume small amounts of power, work with reduced voltages, but also have to be designed efficiently to fit small packages and cost less. These requirements are more demanding as the portable device market is continuously increasing.

A large part of the portable device market is represented by mobile phones, PDAs, laptops, media players, navigation systems (mainly audio-video systems) that use digitally programmable potentiometers (DPP) or digital potentiometers for adjusting the volume, the contrast or the brightness of the display.

1.2 Scope of the doctoral thesis

The purpose of the doctoral thesis is to develop new circuit architectures for improving digital potentiometers performances in audio-video systems. The thesis concentrates on the area reduction with both uniform/linear and fine tuning considered.

Moreover, in order to remove actual limitations of digital potentiometers existing on the market new solutions are proposed. The first limitation refers to the inability to apply voltages higher than the supply on the potentiometer endings. The second one is related to low-voltage applications where potentiometer performances are strongly affected by the small supply values and the power consumption is crucial.

1.3 Content of the doctoral thesis

The doctoral thesis is structured in eight chapters.

In the second chapter, background information related to digital potentiometers is provided.

Chapter 3 treats the digital control section of a DPP. Aspects about the I^2C interface, the most frequently used interface in digital potentiometers, will be presented.

Chapter 4 presents 12 different potentiometers topologies (with one stage and multiple stages) selected from the literature. All configurations designed considering the same conditions are comparatively analyzed through simulations. For the comparison both electrical parameters and consumed area are considered.

Chapter 5 presents the switches, very important components of DPPs, whose characteristics are strongly related to digital potentiometer performances. Different types of switches based on MOS transistors will be compared through simulations.

In chapter 6 two new potentiometers architectures are presented. These two proposed configurations are superior to those described in chapter 4 from both area and linearity characteristics perspectives and this is confirmed by simulations. Furthermore, the experimental results obtained for four I^2C interface digital potentiometers implemented in silicon are exposed. For the silicon implementation of the DPPs, the two best architectures presented in chapter 4 and one of the new configurations (the most linear) were used. For each topology mathematical models were developed in order to determine the theoretical linearity characteristics. These models serve to find the cause of the measured characteristics variations. Based on a set of measurement results, the influence of parasitic layout resistances on the linearity of the potentiometer is emphasized.

Chapter 7 describes two new switches designed to eliminate actual limitations of digital potentiometers. The first switch configuration allows the digital potentiometer to work with voltages higher than the supply. Apart from this feature, the second one facilitates the digital potentiometer low-voltage operation by ensuring performances independent on the supply. Both switches are analyzed by simulations. Additionally, the second configuration, implemented in silicon within a test structure, was tested on the wafer. The measured results for it are also presented in this chapter.

In the last chapter an overview of all the results is done. Here the original contributions brought in the thesis together with the papers where these contributions were exposed will be presented. The last section of this chapter is dedicated to future research perspectives in the digital potentiometers field.

Chapter 2

Digital potentiometers - generalities

2.1 Internal structure

A digital potentiometer (DPP) is an integrated mixed-signal circuit that offers digitally controlled resistances. The internal structure of a DPP comprises the potentiometer architecture itself (the red box in Fig. 2.1) and the digital control section (the green box in Fig. 2.1). The potentiometer architecture is composed of incremental resistances (R0) and switches responsible with delivering the division ratio commanded through the digital interface by an external device (for instance a microcontroller) or the user itself. H and L represent the so-called potentiometer endings for which the maximum applied voltage is limited to the potentiometer supply voltage (V_{CC}), while W is the output terminal called wiper.

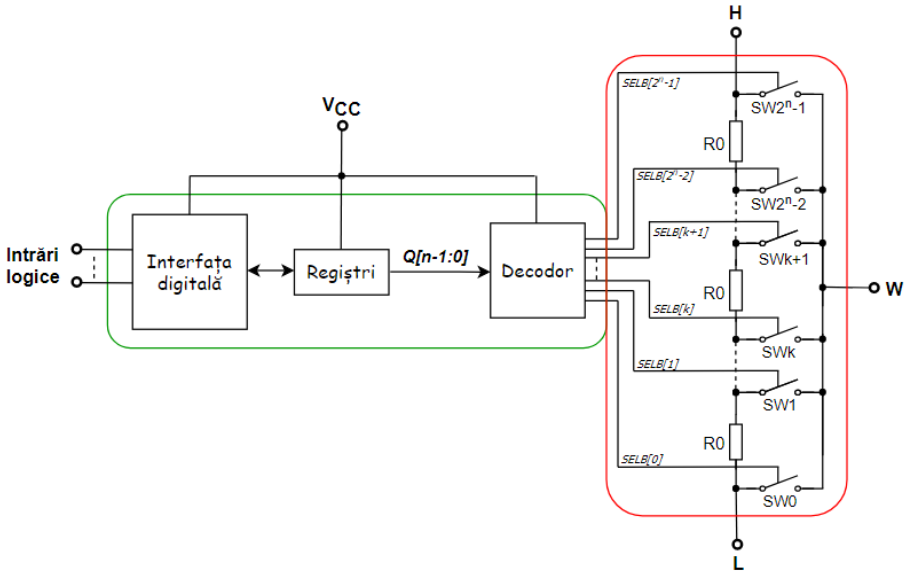


Fig. 2.1 *Schematic bloc of a digital potentiometer.*

2.2 Types of digital potentiometers

Depending on the application to be served, the digital potentiometer can be designed as a voltage divider or rheostat, with linear or logarithmic variation law with respect to the potentiometer step, with volatile or nonvolatile memory, with synchronous or asynchronous digital interface, with one or more than one channels.

2.3 Characteristic parameters

Among the most important parameters of a digital potentiometer, there are: the resolution (a measure of fine-tuning, expressed as the number of bits or steps of the potentiometer), the total resistance (R_{HL}), the wiper resistance R_w (equivalent to the on-state resistance of the switch connecting the resistor ladder), the ZSE and FSE scale errors (which quantify the wiper voltage deviations from ideal values corresponding to zero and the last step) and also the nonlinearity errors: INL (the maximum deviation of the output potentiometer characteristic from the ideal characteristic) and DNL (the maximum deviation between wiper voltages corresponding to two successive steps).

2.4 Typical applications

Digital potentiometers have many applications. Among the most usual there are the televisions, tablets, mobile phones, etc. where DPPs are used for the electronic control of the volume, tone and balance adjustments [1]. They are also commonly used in the LCD displays for brightness control (backlight adjustment), contrast tunning, but also VCOM factory calibration [2].

2.5 Conclusions

Within this chapter general characteristics were presented about digital potentiometers. This section holds the background information needed for understanding the next chapters.

Chapter 3

I^2C digital interface in potentiometers

3.1 Communication protocol

The digital interface represents the connecting element between the external control device and the resistive adjustment section of a digital potentiometer. The most often used in potentiometers is the I^2C synchronous interface. To ensure a successful data transfer, both participants have to comply with a communication protocol. This protocol consists of a set of rules about the transfer initialization, the synchronization between data transfer participants, the data stream control, etc. [3], [4], [5].

3.2 Specific operations in digital potentiometers

The design of the digital interface considers both the rules imposed by the I^2C communication protocol and the digital potentiometer datasheet specifications. In the case of a complex digital potentiometer (having volatile, nonvolatile and write protect registers) the most often operations that can be done through the digital interface are the volatile and nonvolatile registers writing/reading, the write protect instruction, the store operation of the nonvolatile register data into the volatile register and vice versa. Each operation works in a different way and has a different encoding. Those procedures that result in volatile register data modification directly determine the potentiometer step changing.

3.3 Conclusions

In this chapter the functionality of the digital control section of a digital potentiometer having I^2C interface was shown. Here the most usual operations were analyzed through simulations.

Chapter 4

Potentiometers architectures

4.1 Introduction

The most familiar potentiometer architecture is the classic one (as in Fig. 2.1). Although its structure and working principle are very simple, this type of architecture is not cheap at all when fine tunings are needed because of the large area consumed mostly by switches. The solution for implementing cost-efficient high-resolution potentiometers is given by the multistage architectures [6], [7], [8], [9]. Two different categories are described in the literature. The first one uses bulk resistors [6], [8], [9], while the second one uses binary weighted resistors [7].

Four different multistage topologies having bulk resistors (called B0-B3) and seven configurations with binary weighted resistors (denoted by BW1-BW7) are analyzed in this chapter together with the classical architecture. Each architecture was designed in a 0.18µm CMOS technology for a total resistance of 10kΩ and 8 bits of resolution (256 steps). The switch (transfer gate type) used in all configurations was identical. Simulations performed on these topologies allowed a comparative examination of electrical performances (scale errors, linearity characteristics, total resistance variations, wiper resistance). Within the simulations, the voltage applied on the potentiometer endings was considered equal to the supply voltage (V_{HL}=V_{CC}). For each architecture, the consumed area was also estimated.

4.2 Classical architecture – with only one stage

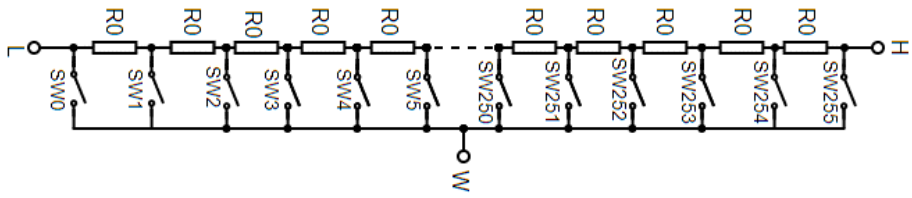


Fig. 4.1 *Electrical schematic of the classical potentiometer architecture (SS) [10], [11].*

4.3 Multistage architectures with bulk resistors

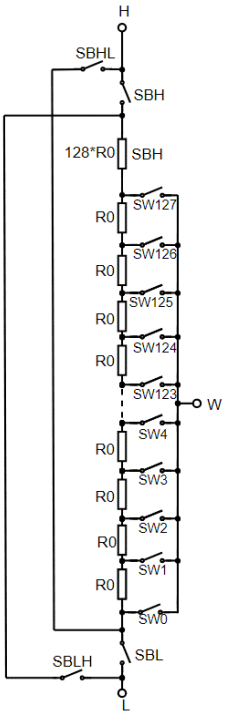


Fig. 4.2 *Electrical schematic of B0 architecture [11].*

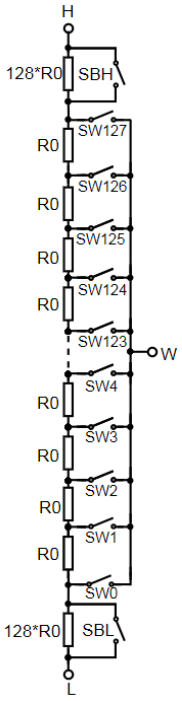


Fig. 4.3 *Electrical schematic of B1 architecture [10], [11].*

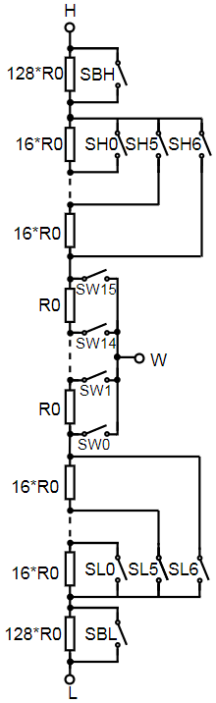


Fig. 4.4 *Electrical schematic of B2 architecture [10], [11].*

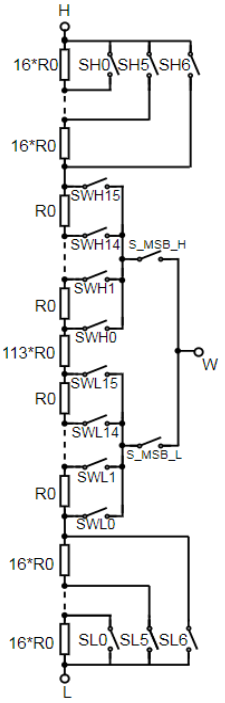


Fig. 4.5 *Electrical schematic of B3 architecture [10], [11].*

4.4 Multistage architectures with binary weighted resistors

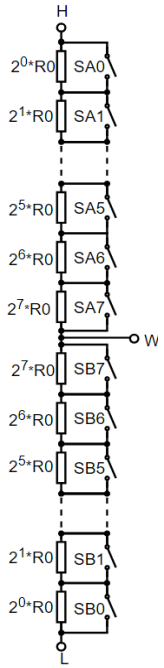


Fig. 4.6 *Electrical schematic of BW1 architecture [10], [11].*

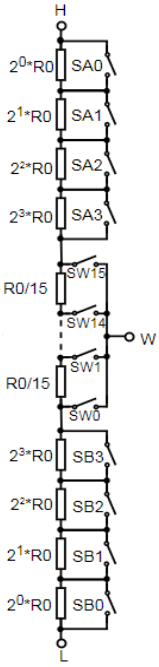


Fig. 4.7 *Electrical schematic of BW2 architecture [10], [11].*

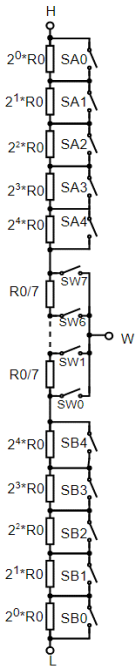


Fig. 4.8 *Electrical schematic of BW3 architecture [10], [11].*

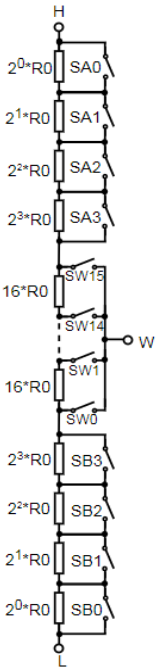


Fig. 4.9 *Electrical schematic of BW4 architecture [11].*

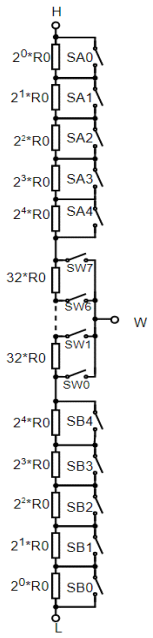


Fig. 4.10 *Electrical schematic of BW5 architecture [11].*

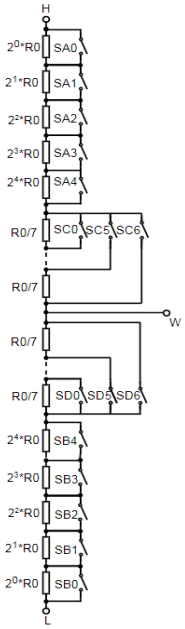


Fig. 4.11 *Electrical schematic of BW6 architecture [11].*

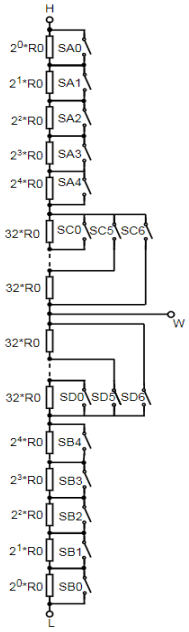


Fig. 4.13 *Electrical schematic of BW7 architecture [11].*

4.5 Studied architectures performances-comparison

The main characteristics of the presented architectures are summarized in Tab. 4.4. In this table there were emphasized those values that are out of the typical datasheet limits of digital potentiometers [12], [13], [14], [15]. The considered limits are: ±1LSB for the INL error, ±0.5LSB for the DNL error, ±0.5LSB for both ZSE and FSE errors, 100Ω for the wiper resistance (R_W) and -100ppm/°C for the total resistance temperature coefficient (TCR).

Tab. 4.1 *Summary of the analyzed architectures performances.*

DPP	Parameter								
	Area [mm²]	|INL| max [LSB]		|DNL| max [LSB]		ZSE [LSB] @2.7V	|FSE| [LSB] @2.7V	R_W max [Ω] @2.7V	TCR max [ppm /ºC]
		@2.7V	@5.5V	@2.7V	@5.5V				
SS	0.2	≈0	≈0	≈0	≈0	0	0	35	-99
B0	0.112	≈0	≈0	≈0	≈0	0.239	0.204	35	-97
B1	0.111	0.150	0.074	0.296	0.165	0.239	0.204	35	-98
B2	0.037	0.830	0.044	**1.470**	0.112	0.474	0.405	35	-96
B3	0.046	0.200	0.084	0.290	0.164	0.236	0.201	70	-98
BW1	0.027	**1.100**	0.530	**1.244**	**0.880**	**1.812**	**1.556**	0	-89
BW2	0.024	**1.020**	0.970	**1.620**	**1.160**	**0.950**	**0.810**	35	-94
BW3	0.026	**1.025**	0.520	**1.230**	**0.700**	**1.189**	**1.008**	35	-95
BW4	0.026	**1.020**	0.998	**1.650**	**1.170**	**0.864**	**0.747**	35	-95
BW5	0.022	**1.410**	0.815	**1.550**	**0.900**	**1.099**	**0.948**	35	-94
BW6	0.044	**0.920**	0.885	**0.970**	**0.990**	**1.384**	**1.185**	0	-91
BW7	0.033	**1.310**	0.776	**1.440**	**0.850**	**1.336**	**1.150**	0	-91

According to Tab. 4.1 the topologies having binary weighted resistors (BW1-BW7) are the most cost-efficient since they occupy very small areas. In particular BW5 consumes the smallest area. The SS configuration is the best choice when it comes to both nonlinearity and scale errors. This happens because on the H to L path there is no switch to introduce unwanted resistors (see Fig. 4.1). Though, the large area of the SS topology (almost ten times larger than the smallest area) makes it a very expensive architecture for the design of 8-bits resolution digital potentiometers. The highest errors (INL>0.9LSB, DNL>0.5LSB, FSE>0.7LSB, ZSE>0.8LSB) correspond to multistage architectures with binary weighted resistors, particularly for small supply volatages (2.7V).

The compromise solution considering both area and errors is that of multistage architectures having bulk resistors. For large supply voltages (5.5V), B2 configuration is the best choice because of its small nonlinearity errors (INL<0.05, DNL<0.12) and small area (0.037mm^2). In turn, for small voltages (2.7V), B3 architecture is superior to B2. Its corresponding DNL error (0.29LSB) is significantlly smaller than the value corresponding to B2 (1.47LSB). The price paid for using B3 configuration instead of B2 is the double wiper resistance value and slightly larger area (0.046mm^2).

4.6 Conclusions

To conclude, for the design of cheap and performant digital potentiometers (with fine and uniform tuning) used in audio-video systems the best configurations are B2 and B3.

Chapter 5

Switches

5.1 Generalities

A switch is an electronic circuit having two states. In the ON state it allows the current to pass, but a small resistance called on-resistance (R_{ON}) is opposed to the current flow. In the OFF state, the circuit is interrupted and a very small amount of current called off-state leakage current (I_{OFF}) is flowing through the switch. The smaller these two parameters, the more performant the switches.

5.2 Switches purpose in digital potentiometers

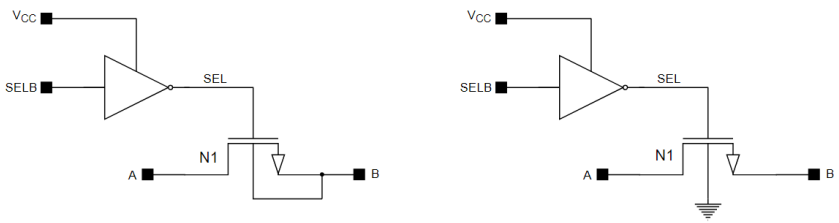
Switches represent important elements of digital potentiometers. Their characteristics are strongly affecting DPPs performances.

The on-resistance is the most restrictive parameter. It impacts the wiper resistance, but also the nonlinearity and scale errors of multistage architectures. Additionally, R_{ON} establishes the minimum supply voltage of the potentiometer. It also sets up the voltage range that can be applied on H and L terminals.

The off-state leakage current significantly contributes to the power consumption of a high-resolution digital potentiometer.

The switch bidirectionality offers more flexibility to the potentiometer within the application.

5.3 nMOS switch



a) b)

Fig. 5.1 *Electrical schematic of the nMOS switch: a) unidirectional version; b) bidirectional version.*

5.4 pMOS switch

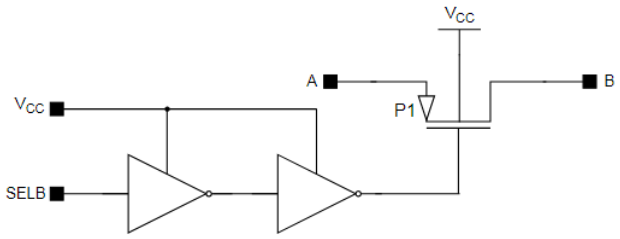


Fig. 5.2 *Electrical schematic of the pMOS switch.*

5.5 CMOS switches

By parallel connecting an nMOS transistor with a pMOS transistor, the transfer gate or CMOS switch configuration results. In the following sections there will be analyzed 3 versions of CMOS switches. The difference between them consists of the way the switching devices substrate polarization is done.

5.5.1 CMOS I

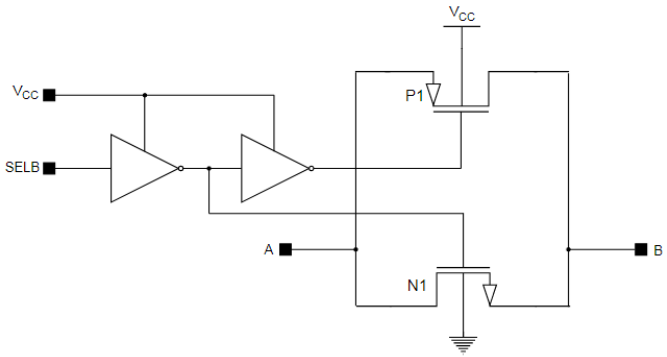


Fig. 5.3 *Electrical schematic of the CMOS I switch.*

5.5.2 CMOS II

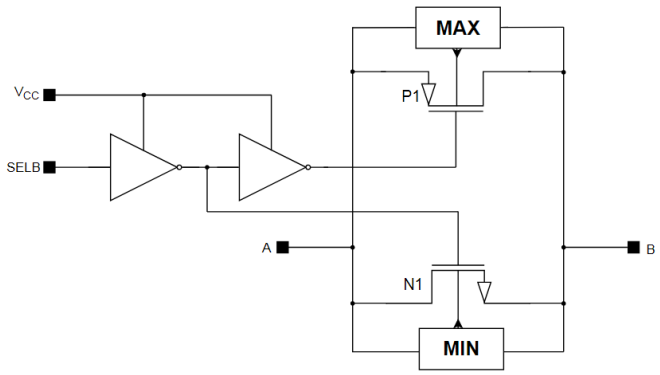


Fig. 5.4 *Electrical schematic of the CMOS II switch.*

5.5.3 CMOS III

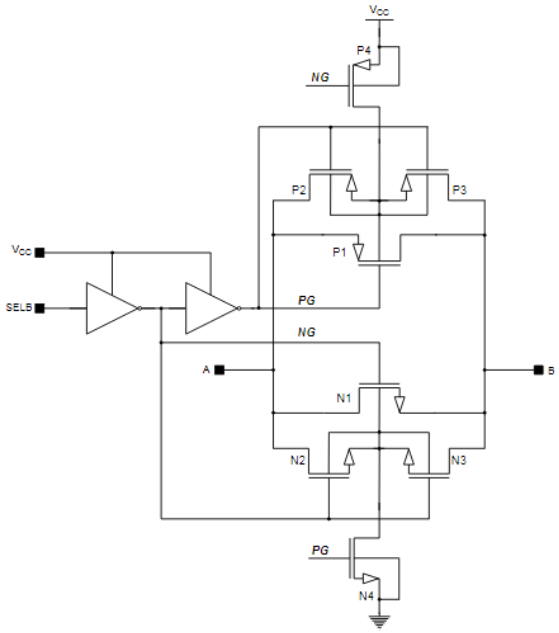


Fig. 5.5 *Electrical schematic of the CMOS III switch.*

5.6 Conclusions

Within this chapter several switches based on MOS transistors were analyzed through simulations. These were designed in a 0.18µm 5V CMOS technology considering the criterion of maximum 100Ω on-resistance for V_{CC}=2.7V, process variations and three temperatures (-40°C, 25°C, 85°C). The first exposed switch was that made of an nMOS transistor. For this one both unidirectional and bidirectional configurations were presented. For the other types of switches (pMOS and CMOS) only the bidirectional version was considered. In Tab. 5.2 the performances of all bidirectional switches are summarized.

Tab. 5.1 *Summary of the analyzed bidirectional switches performances.*

	nMOS	**pMOS**	**CMOS I**	**CMOS II**	**CMOS III**
V_A range for which R_{ON}<100Ω @ V_{CC}=2.7V	<1.34V	>1.4V	0÷V_{CC}	0÷V_{CC}	0÷V_{CC}
Consumed area [µm²]	1190	4490	5650	1600	1660
I_{OFF} max [nA]	6	200	200	22	22

Because the on-resistance criterion is met for the whole range 0÷V_{CC} only for CMOS switches, these ones are the most recommended in the digital potentiometer design. Among CMOS switches, CMOS II and III occupy the smallest area. These two versions also have the smallest off-state leakage current. Both performances are a consequence of using actual techniques for the switching devices substrate biasing to ensure substrate-source voltages close to zero (inspired from patent [16]).

Chapter 6

New digital potentiometers architectures; Experimental results

6.1 Introduction

In this chapter, two new potentiometer architectures will be presented. These two configurations are derived from the B2 topology. Their linearity and area performances are superior to all architectures presented in chapter 4. One of the proposed architectures (denoted by B4D) was used together with B2 and B3 configurations in the silicon implementation of 8-bits digital potentiometers. For supply voltages in the range of 2.7V-5.5V and three temperatures (-40°C, 25°C and 85°C) the following parameters were measured: the total resistance of the potentiometer, the wiper resistance and the nonlinearity errors. The usual datasheet specification limits were considered for these parameters: ±20% and -100ppm/°C for total resistance tolerance and TCR, 100Ω for the wiper resistance, ±1LSB and ±0.5LSB for the INL and DNL errors.

6.2 B2 architecture

6.2.1 Layout

The B2 configuration (Fig. 4.4) was used in the silicon manufacturing (in a 0.5µm CMOS process) of a dual volatile DPP having a total resistance of 50kΩ and I^2C interface. Its drawn layout is shown in Fig. 6.1.

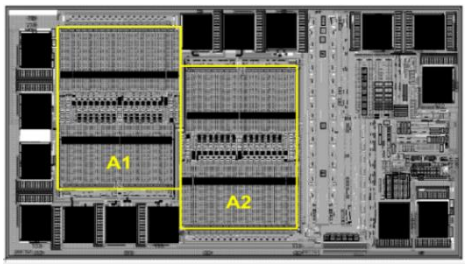


Fig. 6.1 *The layout of the dual DPP implemented in silicon using architecture B2 [17].*

6.2.2 Total resistance

The maximum value for the total resistance tolerance is 7% while its temperature coefficient of resistance, specific to the technology, is −170 ppm/ºC.

6.2.3 Wiper resistance

Wiper resistance (R_W) variations with the step are represented in Figs. 6.3-6.4 for V_{CC}=2.7V and 5.5V, respectively.

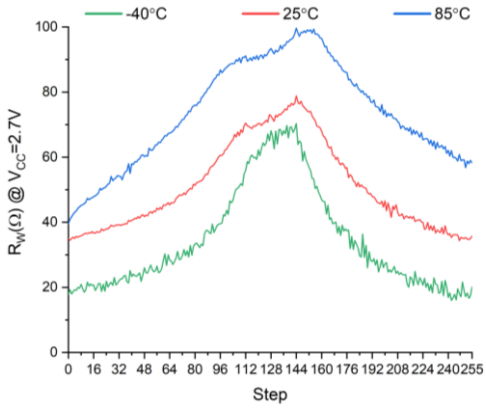


Fig. 6.2 *Wiper resistance measured variation with step for the B2 architecture-based silicon implemented DPP when V_{CC}=2.7V.*

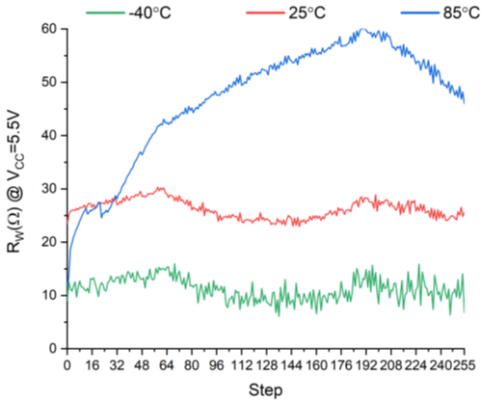


Fig. 6.3 *Wiper resistance measured variation with step for the B2 architecture-based silicon implemented DPP when V_{CC}=5.5V.*

It can be observed that the largest values for R_W correspond to 85ºC: 100Ω for V_{CC}=2.7V (Fig. 6.3) and 60Ω for V_{CC}=5.5V (Fig. 6.4).

6.2.3 Linearity characteristics

The measured linearity characteristics for the B2 architecture-based silicon implemented DPP are given in Figs. 6.5-6.8. The maximum value for INL error is -0.4LSB for V_{CC}=2.7V (Fig. 6.5) and -0.35LSB for V_{CC}=5.5V (Fig. 6.6). For DNL error the peak value corresponds to -0.4LSB for both supply voltages (Figs. 6.7-6.8).

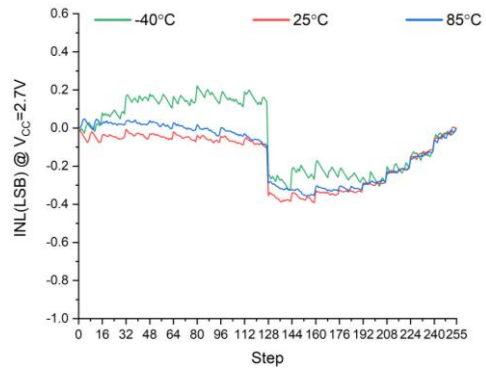


Fig. 6.4 *Measured INL error variation with step for the B2 architecture-based silicon implemented DPP when V_{CC}=2.7V [17].*

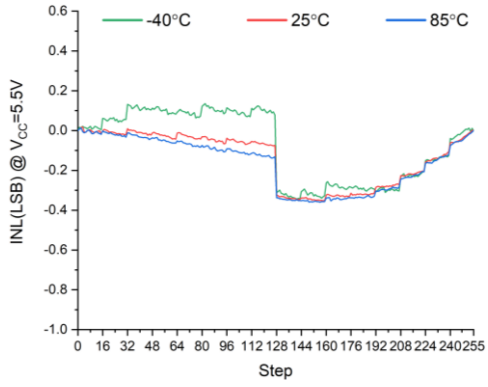


Fig. 6.5 *Measured INL error variation with step for the B2 architecture-based silicon implemented DPP when V_{CC}=5.5V.*

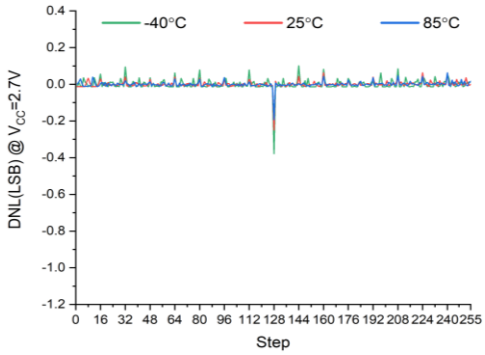


Fig. 6.6 *Measured DNL error variation with step for the B2 architecture-based silicon implemented DPP when V_{CC}=2.7V [17].*

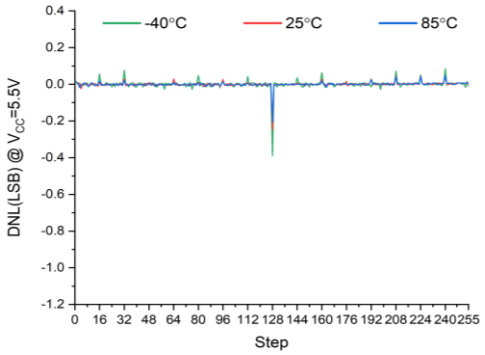


Fig. 6.7 *Measured DNL error variation with step for the B2 architecture-based silicon implemented DPP when V_{CC}=5.5V.*

To explain the experimental linearity characteristics, a mathematical model has been developed for expressing the wiper voltage as a function of the on-resistances of the switches bypassing resistors on H to L path (see Fig. 4.4) and the incremental resistance (R0) deviations expressed for each stage of B2 architecture (see Fig. 4.4). Based on this modeled wiper voltage, the theoretical variations with step of INL and DNL errors were determined considering two cases. The variations obtained for the first case (when R0 deviations were zero) are given in Fig. 6.9. When certain values are considered for the R0 deviations (second case), INL and DNL theoretic errors (red plots in Fig. 6.10) get close to measured ones (blue plots in Fig. 6.10). It thus gets confirmed that both on-resistance and incremental resistance deviations are responsible with the linearity characteristics degradation of this DPP.

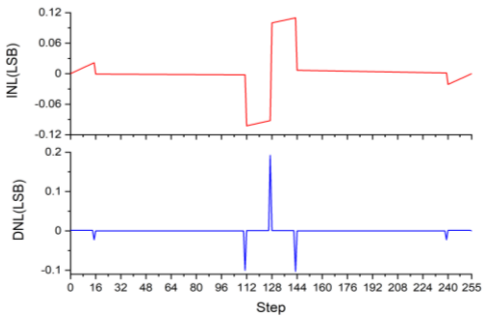


Fig. 6.8 *INL and DNL theoretical variations with step for B2 architecture when no incremental resistance deviations exist.*

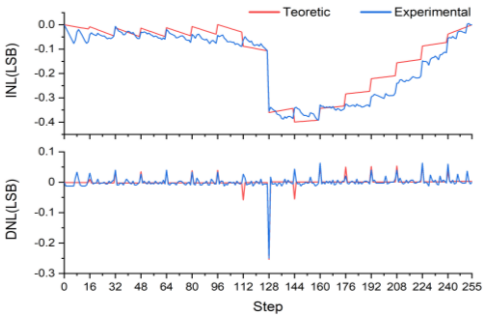


Fig. 6.9 *INL and DNL theoretical variations with step for B2 architecture when incremental resistance deviations exist vs. measured variations.*

6.3 B3 architecture

6.3.1 Layout

The B3 architecture (Fig. 4.5) was used for the silicon implementation in a 0.5µm EEPROM process of a 50kΩ nonvolatile DPP with I^2C interface (with drawn layout given in Fig. 6.11).

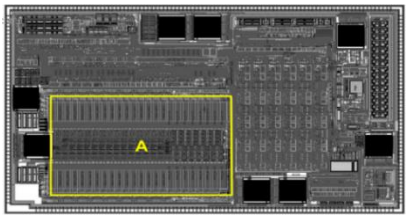


Fig. 6.10 *The layout of the DPP implemented in silicon using architecture B3 [17].*

6.3.2 Total resistance

The maximum measured tolerance for R_{HL} is 5%. Compared with the previous DPP built using the B2 architecture, the TCR is smaller (-140 ppm/ºC), so the technology is more stable.

6.3.3 Wiper resistance

In Figs. 6.13-6.14 the measured wiper resistance variations with step for V_{CC}=2.7V and 5.5V are given.

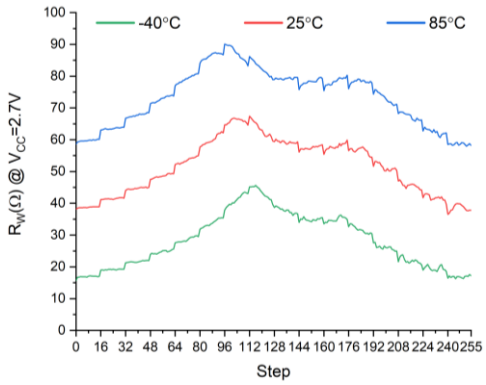


Fig. 6.11 *Wiper resistance measured variation with step for the B3 architecture-based silicon implemented DPP when V_{CC}=2.7V.*

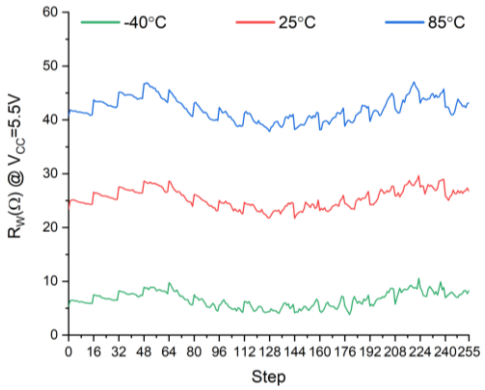


Fig. 6.12 *Wiper resistance measured variation with step for the B3 architecture-based silicon implemented DPP when V_{CC}=5.5V.*

The largest values for R_W correspond to 85ºC: 90Ω for V_{CC}=2.7V (Fig. 6.13) and 47Ω for V_{CC}=5.5V (Fig. 6.14). These maximum values are comparable with those obtained for the DPP implemented in silicon using B2 topology, but the switch (CMOS I) area is twice larger.

6.3.4 Linearity characteristics

The measured linearity characteristics for B3 architecture-based silicon implemented DPP are depicted in Figs. 6.15-6.18. The maximum value for INL error reaches the limit of -1LSB for both V_{CC}=2.7V (Fig. 6.15) and V_{CC}=5.5V (Fig. 6.16). As it concerns the DNL error, the peak values correspond to -1.2LSB (far larger than the ±0.5LSB limit) for both supply voltages (Figs. 6.17-6.18).

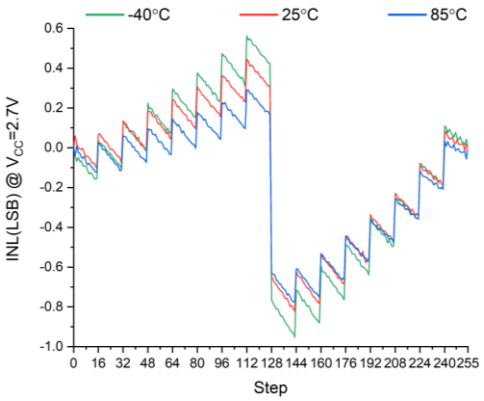


Fig. 6.13 *Measured INL error variation with step for the B3 architecture-based silicon implemented DPP when V_{CC}=2.7V [17].*

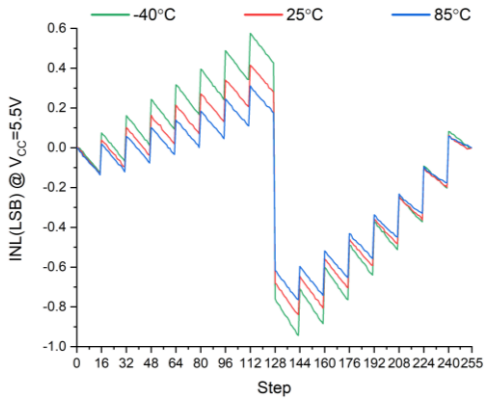


Fig. 6.14 *Measured INL error variation with step for the B3 architecture-based silicon implemented DPP when V_{CC}=5.5V.*

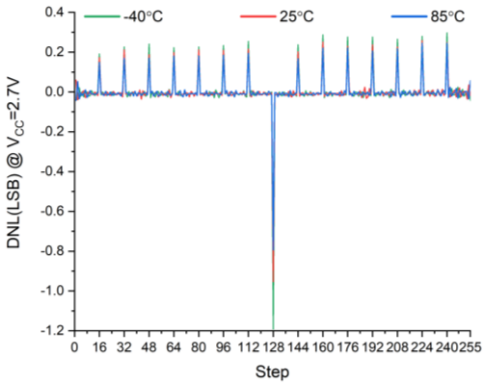


Fig. 6.15 *Measured DNL error variation with step for the B3 architecture-based silicon implemented DPP when V_{CC}=2.7V [17].*

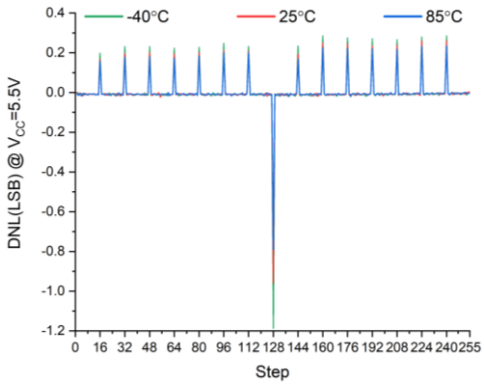


Fig. 6.16 *Measured DNL error variation with step for the B3 architecture-based silicon implemented DPP when V_{CC}=5.5V.*

In order to identify the determining factor for the measured nonlinearity errors variations, a mathematic model is also proposed for the B3 architecture, based on the same principle used for the B2 configuration. When no incremental resistance deviations exist, the resulting INL and DNL errors variations are exposed in Fig. 6.19. It can be noticed that these theoretical values are much smaller than the measured ones (at least one order of magnitude smaller). When certain R0 deviations are considered for each stage of the B3 configuration, the theoretical linearity characteristics almost perfectly match those measured (Fig. 6.20).

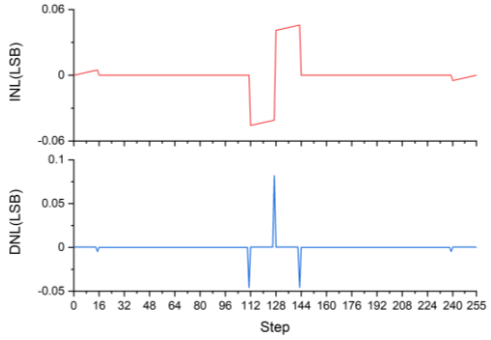


Fig. 6.17 *INL and DNL theoretical variations with step for B3 architecture when no incremental resistance deviations exist.*

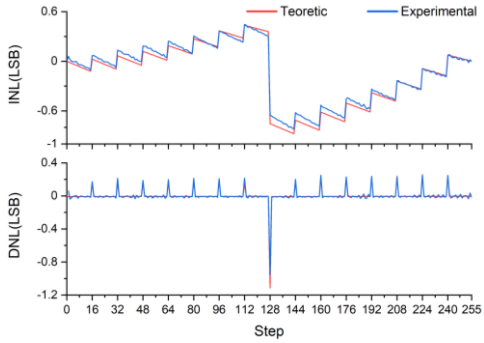


Fig. 6.18 *INL and DNL theoretical variations with step for B3 architecture when incremental resistance deviations exist vs. measured variations.*

Although the on-resistances of the switches used in the B2 and B3 architecture-based DPPs are comparable (see Figs. 6.13-6.14 vs. 6.3-6.4), the B3 architecture, considered superior to B2 for low voltages in chapter 4, loses this advantage because of the incremental resistance deviations.

6.4 Multistage potentiometer architectures with improved linearity

6.4.1 B4 architecture

The B4 architecture is derived from B2 topology presented in chapter 4. The bulk resistors of 128*R0 (see Fig. 4.4) were split into 8 blocks of 16*R0 which were included in the shunt stages. The B4 configuration resulting schematic is displayed in Fig. 6.21. This new topology eliminates the errors caused by the different biasing of shunt stages switches in the B2 architecture case. This is confirmed by the simulations (done in the same conditions as those in chapter 4), which are exposed in Fig. 6.22. The B4 architecture maximum absolute errors are significantly reduced compared to those corresponding to the B2 configuration (from 0.8LSB to 0.015LSB for INL, and from 1.47LSB to 0.015LSB for DNL). It should be mentioned that B4 topology area is larger than that of B2 (0.049mm^2 compared to 0.037mm^2) due to more switches needed in the B4 structure. Moreover, the linearity performances of B4 configuration are even better than those offered by the B3 topology (see Tab. 4.4).

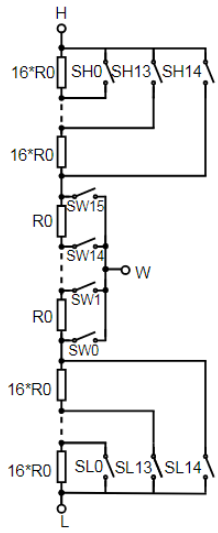


Fig. 6.19 *Electrical schematic of B4 architecture [18].*

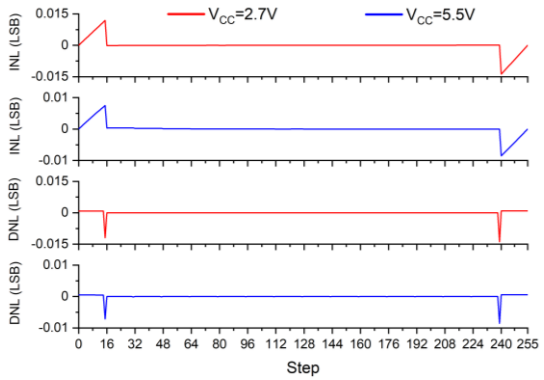


Fig. 6.20 *Simulated INL and DNL errors variations with step for B4 architecture when V_{CC}=2.7V and 5.5V.*

6.4.2 B4D architecture

Adding compensation structures in the shunt stage [6] of B4 architecture results in B4D configuration whose schematic is given in Fig. 6.23. These structures help in reducing even more the nonlinearity errors by keeping constant the potentiometer total equivalent resistance regardless the step. The simulations done on B4D architecture attest its superiority. The maximum absolute value is now 0.0005LSB (Fig. 6.24) compared to 0.015LSB obtained for the B4 topology errors. In addition, the B4D architecture is less affected by the switch's dimensions.

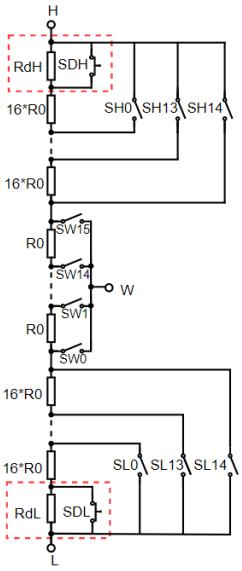


Fig. 6.21 *Electrical schematic of B4D architecture [18].*

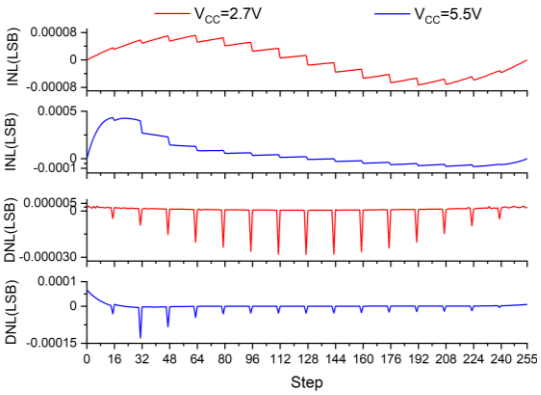


Fig. 6.22 *Simulated INL and DNL errors variations with step for B4D architecture when V_{CC}=2.7V and 5.5V.*

6.5 B4D architecture - experimental results

The B4D proposed configuration, presented in the previous paragraph, was used in the silicon implementation of two digital potentiometers manufactured in two different technologies: 0.18µm CMOS and 0.18µm EEPROM.

6.5.1 Layout B4D CMOS

At first, the B4D topology was used for the fabrication in a 0.18µm CMOS process of a 50kΩ volatile DPP with I^2C interface (with drawn layout in Fig. 6.26).

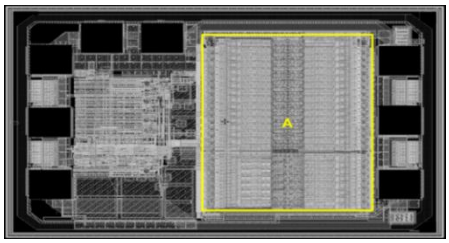


Fig. 6.23 *The layout of the DPP implemented in silicon using architecture B4D CMOS.*

6.5.2 Total resistance B4D CMOS

The maximum measured tolerance value for the total resistance of this DPP is 4%. Typical to the technology, the R_{HL} TCR is about -320 ppm/ºC, double compared to that obtained for the silicon implemented DPPs with B2 and B3 architectures.

6.5.3 Wiper resistance B4D CMOS

The measured wiper resistance variations with the step are shown in Fig. 6.28-6.29. The largest R_W values correspond to -40ºC for V_{CC}=2.7V (325Ω) (see Fig. 6.28), and 85ºC for V_{CC}=5.5V (10Ω) (see Fig. 6.29). Because the reference value of

100Ω is exceed even for 25ºC, this DPP is not recommended in low voltage applications. In turn, for high voltages (V_{CC}=5.5V) the wiper resistance has the smallest value compared to B2 and B3 previously exposed measurements.

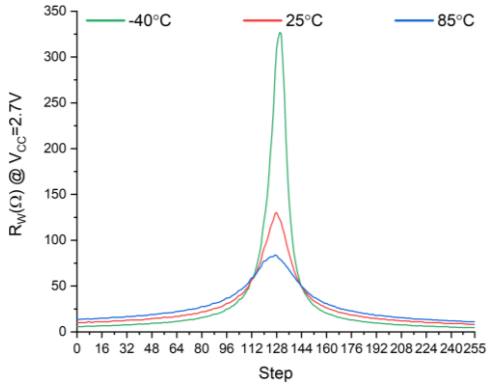


Fig. 6.24 *Wiper resistance measured variation with step for the B4D CMOS architecture-based silicon implemented DPP when V_{CC}=2.7V.*

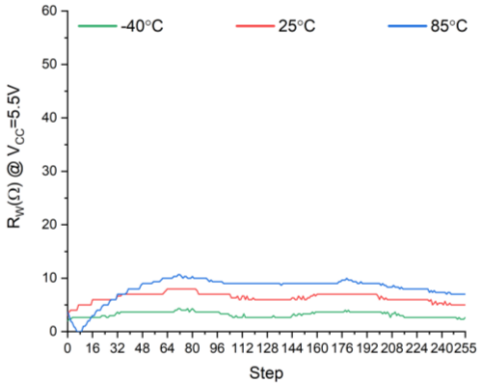


Fig. 6.25 *Wiper resistance measured variation with step for the B4D CMOS architecture-based silicon implemented DPP when V_{CC}=5.5V.*

6.5.4 Linearity characteristics B4D CMOS

The INL and DNL measured variations with the potentiometer step are exposed in Figs. 6.30-6.33. The maximum INL value is about -0.3LSB (Figs. 6.30-6.31), while maximum DNL reaches -0.13LSB (Figs. 6.32-6.33). Compared to previous DPPs, the smallest nonlinearity errors are met for B4D CMOS based DPP.

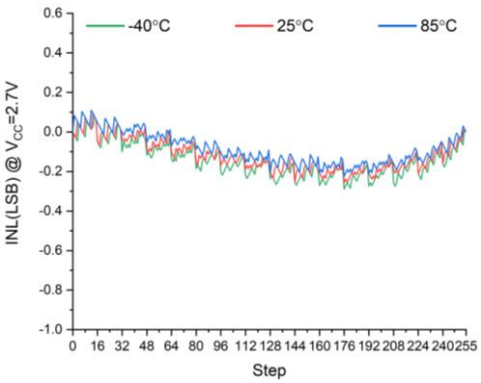


Fig. 6.26 *Measured INL error variation with step for the B4D CMOS architecture-based silicon implemented DPP when V_{CC}=2.7V.*

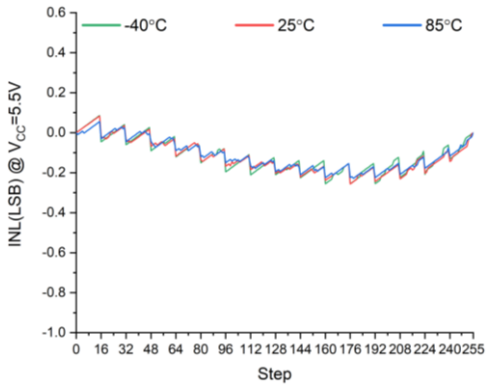


Fig. 6.27 *Measured INL error variation with step for the B4D CMOS architecture-based silicon implemented DPP when V_{CC}=5.5V [18].*

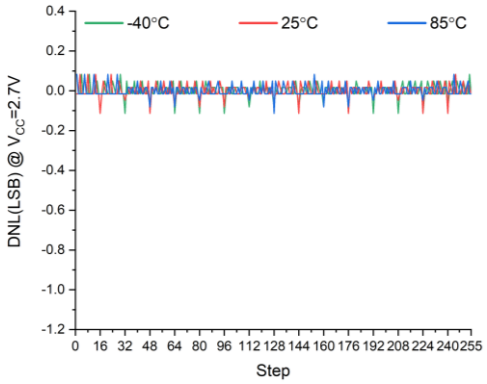


Fig. 6.28 *Measured DNL error variation with step for the B4D CMOS architecture-based silicon implemented DPP when V_{CC}=2.7V.*

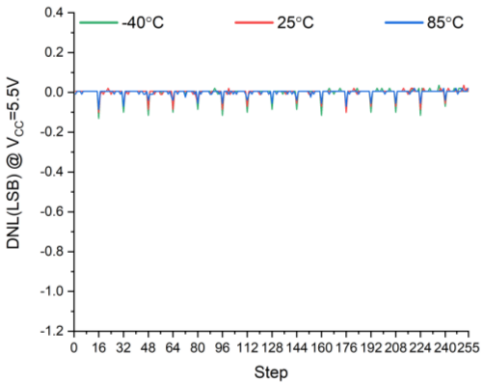


Fig. 6.29 *Measured DNL error variation with step for the B4D CMOS architecture-based silicon implemented DPP when V_{CC}=5.5V [18].*

The mathematic model developed on the same principle as that used for B2 and B3 architecture-based DPPs, proved that when no incremental resistance variations exist the nonlinearity errors are zero. So, the measured linearity characteristics are exclusively caused by R0 variations. This statement is confirmed by the matching between the theoretical/simulated curves (both obtained for certain nonzero R0 deviations) and the measured curves, all gathered in Fig. 6.34.

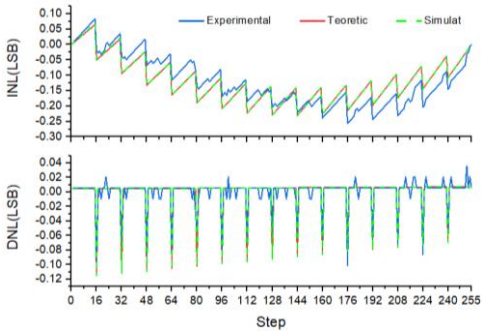


Fig. 6.30 *Theoretical and simulated INL and DNL errors variations with step when incremental resistance deviations exist vs. measured variations for B4D CMOS architecture when V_{CC}=5.5V [18].*

6.5.5 Layout B4D EEPROM

The new B4D architecture was also used for the silicon implementation in a 0.18µm EEPROM technology of a nonvolatile 10kΩ DPP with I^2C interface. The drawn layout of this DPP is shown in Fig. 6.35.

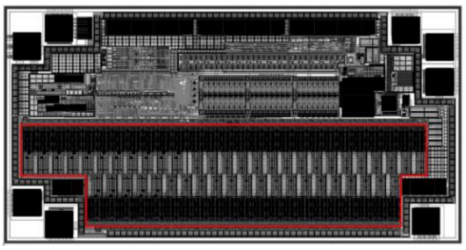


Fig. 6.31 *The layout of the DPP implemented in silicon using architecture B4D EEPROM [19].*

6.5.6 Linearity characteristics B4D EEPROM

The measured linearity characteristics for the B4D based DPP implemented in the EEPROM technology are given in Figs. 6.36-6.37 for V_{CC}=5.5V and 25ºC.

Compared with the corresponding nonlinearity errors of the DPP implemented with the same architecture (B4D) but in a CMOS technology (see the red plots exposed in Figs. 6.31 and 6.33), in the waveforms shown in Figs. 6.36-6.37 some additional bounces and spikes appear regularly for particular steps. The cause of this unexpected behavior, confirmed by the simulations shown in Figs. 6.41-6.42, is the parasitic resistance (of about 3.4Ω) of an interconnecting wire existing in the wiper stage layout of the B4D EEPROM architecture.

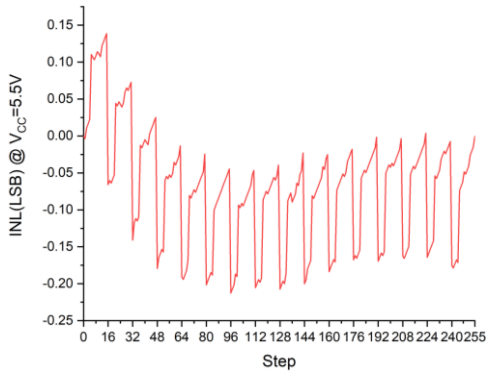


Fig. 6.32 *Measured INL error variation with step for the B4D EEPROM architecture-based silicon implemented DPP [19].*

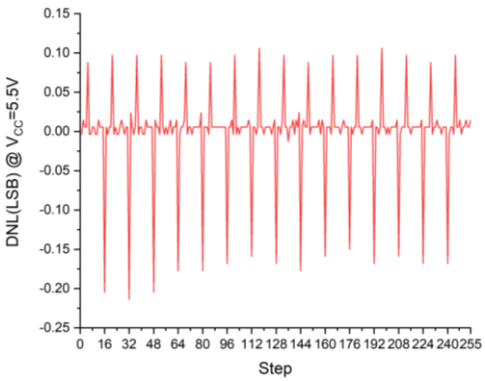


Fig. 6.33 *Measured DNL error variation with step for the B4D EEPROM architecture-based silicon implemented DPP [19].*

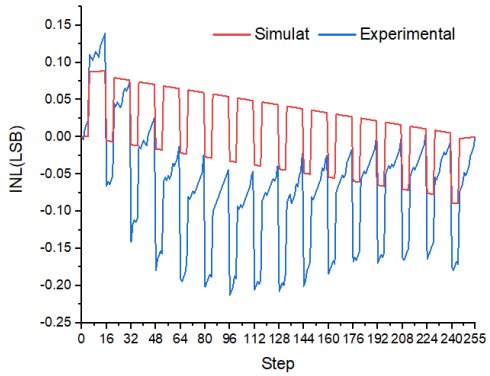


Fig. 6.34 *Simulated INL error variation with step when the parasitical resistance (R_P=3.4Ω) is introduced in the B4D architecture wiper stage vs. measured variation [19].*

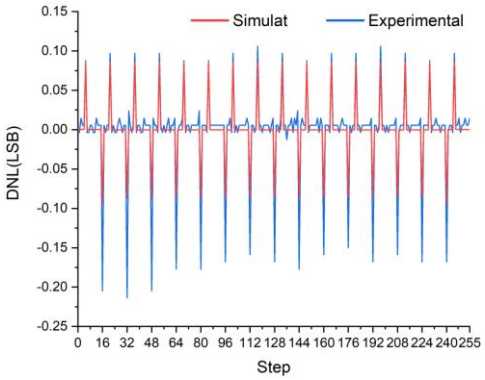


Fig. 6.35 *Simulated DNL error variation with step when the parasitical resistance (R_P=3.4Ω) is introduced in the B4D architecture wiper stage vs. measured variation [19].*

To conclude, for the design of highly linear DPPs, the layout of the architecture itself has a tremendous importance. It should be as compact as possible and have minimum length interconnecting wires.

6.6 Comparison between B2, B3, B4D CMOS architectures

In order to carry out a comparative analysis of the exposed 50kΩ DPPs, their characteristics are summarized in Tab. 6.6. For most of the parameters there were added the common limits from digital potentiometers datasheets.

Tab. 6.1 *50kΩ experimental analyzed DPPs performances.*

Parameter	Common Limit	B2 Architecture	B3 Architecture	B4D CMOS Architecture
DPP type	-	volatile	nonvolatile	volatile
Technology	-	0.5µm CMOS	0.5µm EEPROM	0.18µm CMOS
Area[mm^2]	-	1.25	3.9	0.49
R_{HL} Tolerance [%]	*20*	7	5	4
R_{HL} TCR [ppm/°C]	*100*	-170	-140	-320

R_W max @V_{CC}=2.7V [Ω]	*100*	100	90	325
R_W max @V_{CC}=5.5V [Ω]	*100*	60	47	10
INL max [LSB]	*±1*	-0.4	-1	-0.3
DNL max [LSB]	*±0.5*	-0.4	-1.2	-0.13

6.7 Conclusions

Within this chapter there were proposed two new architectures (B4 and B4D) derived from the B2 configuration presented in chapter 4. These new topologies are superior from the perspective of area and linearity to all architectures studied in chapter 4. Additionally, the experimental results obtained for four digital potentiometers implemented using the B2, B3 and B4D architectures were exposed and analyzed. The best linearity characteristics correspond to B4D topology and this was proven by simulations, but also by theoretical and experimental results. If its layout is carefully done (considering matching techniques, minimum interconnections), then the linearity performances of a DPP designed using the proposed B4D architecture is conditioned only by technological limitations.

Chapter 7

Switches for digital potentiometers with improved performances

7.1 CMOS switch with extended range over the supply voltage

The proposed bidirectional CMOS switch with extended voltage over the supply [20] has the schematic shown in Fig. 7.1. It consists of two p-type (P1 and P2) and two n-type (N1 and N2) switching transistors. Their substrate biasing technique is different from those exposed in chapter 5, but the purpose is the same (to keep V_{BS} as close as possible to zero). The level-shifter (LS) blocks from the switch structure (Fig. 7.1) play crucial roles in the OFF state. They translate the P1 and P2 command level from V_{CC} to V_A and V_B values in order to keep these transistors turned off when the voltage applied on the switch exceeds V_{CC}. In the patent [21] an electrical schematic of bidirectional switch having extended voltage range is also described.

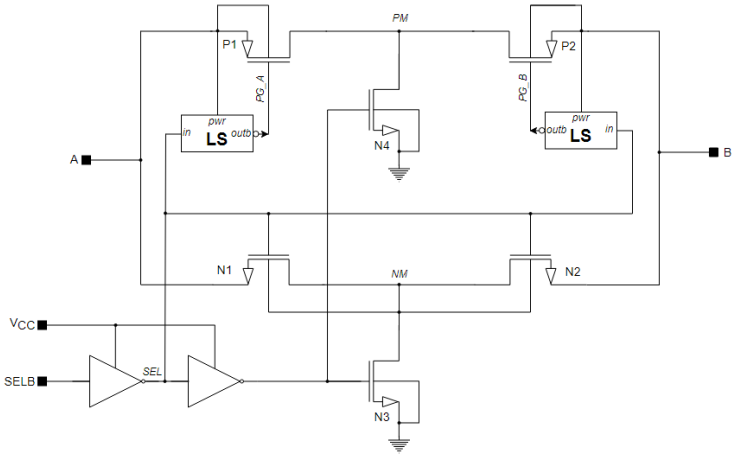


Fig. 7.1 *Electrical schematic of the CMOS switch with extended range over the supply voltage [20].*

The efficiency in using the LS blocks is confirmed by the simulations (Fig. 7.3). In their absence, for V_{CC}=2.7V and V_A>3.3V a large amount of current (on the order of mA, Fig. 7.3c)) pass through the switch in the OFF state. When these LS

blocks are employed (schematic shown in Fig. 7.1), the maximum off-state leakage current is about 50nA (Fig. 7.3a)).

The same technology (0.18µm 5V CMOS) and criterion as those used for the switches in chapter 5 are considered for the design of the CMOS switch with extended range over the supply voltage. The resulted area needed for ensuring the R_{ON} max of 100Ω when V_{CC}=2.7V (Fig. 7.4) is 4300µm^2.

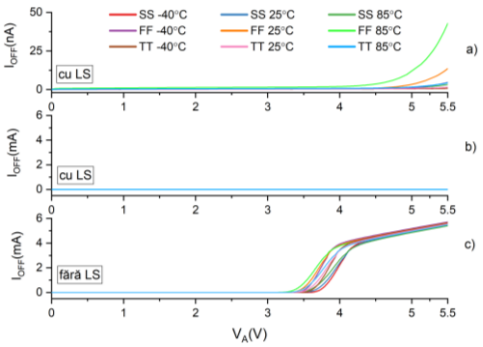


Fig. 7.2 *The off-state leakage current (I_{OFF}) for the CMOS switch with extended range over the supply voltage when V_{CC}=2.7V:*
a) with LS blocks included in the schematic (zoom);
b) with LS blocks included in the schematic;
c)without LS blocks.

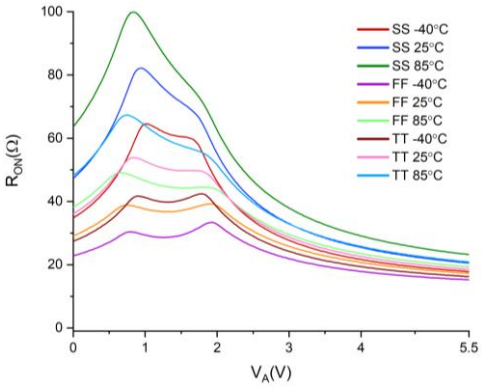


Fig. 7.3 *R_{ON} variation with V_A for the CMOS switch with extended range over the supply voltage.*

Compared to the CMOS versions studied in chapter 5, the area consumed by the CMOS switch with extended range over the supply voltage is larger than that of CMOS II and III, but smaller than CMOS I. This new proposed switch is also superior to CMOS I with respect to I_{OFF} (see Tab. 5.2). But it is important to bear in mind that only the proposed switch (Fig. 7.1) is capable of operating with voltages higher than the supply. This defining characteristic allows the digital potentiometer to work with voltages over its supply.

7.2 Nonvolatile switch

7.2.1 Nonvolatile switch structure and functionality

The second proposed switch is the unidirectional nonvolatile switch with the schematic given in Fig. 7.9. This consists of a switching nMOS floating gate transistor (NSW in Fig. 7.9) and a memory cell responsible with FGR floating gate programming.

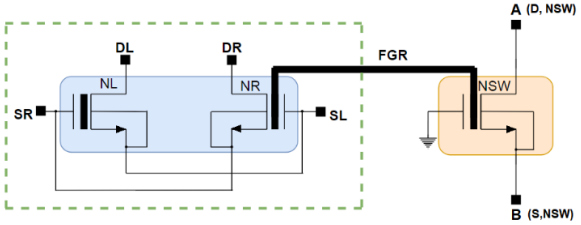
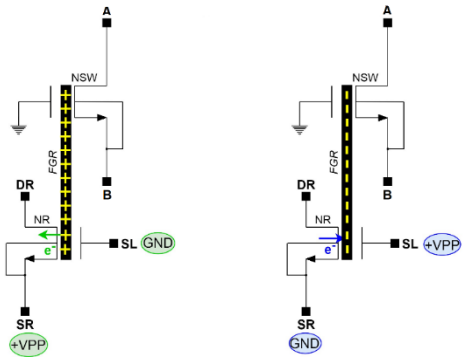


Fig. 7.4 *Electrical schematic of the nonvolatile switch [22], [23].*

One distinguished characteristic of the nonvolatile switch is that, unlike standard switches, its command voltage (V_{FGR}) is programmable and independent of the supply voltage. This feature makes this kind of switch very suitable in low-voltage applications, where performances are limited due to the small supply voltages. Actual methods used in such applications rise the command voltage, but to some values dependent on the supply [24-28]. Additionally, due to its nonvolatile nature, after the switch gets programmed, it does not consume current.

The ON and OFF state programming of the switch happens whenever proper programming voltage (VPP) is applied on the memory cell, according to Fig. 7.10.

The corresponding drawn layout of the nonvolatile switch occupies 2400μm^2 (Fig. 7.11). It was included into a silicon implemented test structure in a 0.18μm EEPROM technology.



a) b)

Fig. 7.5 *NSW programming conditions a) ON and b) OFF [23].*

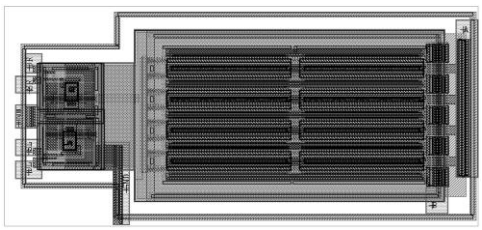


Fig. 7.6 *Nonvolatile switch drawn layout [22].*

7.2.2 Experimental results

Wafer measurements done on the test structure have shown important features of the nonvolatile switch. The first thing is that the nonvolatile switch inherent state is OFF. It can be repeatedly programmed ON and OFF through the memory cell biasing with proper programming voltages. Once programmed the nonvolatile switch retain its state.

Moreover, the NSW drain current variation with the voltage source (Fig. 7.18) revealed a dependency of the command voltage V_{FGR} on the programming voltage (VPP) in accordance with the data exposed in Tab. 7.3.

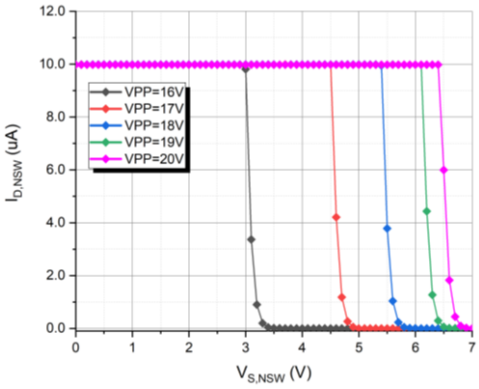


Fig. 7.7 *Measured NSW drain current variation with $V_{S,NSW}$ for different VPPs [23].*

Tab. 7.1 *V_{FGR} (VPP) dependency.*

VPP (V)	$V_{S,NSW}$ (V)	V_{FGR} (V)
16	3	3.9
17	4.5	5.4
18	5.4	6.3
19	6.1	7
20	6.4	7.3

The measured on-resistance of the nonvolatile switch varies between 45Ω and 70Ω for source voltages below 2V (Fig. 7.21) after VPP=18V was applied on the memory cell for the ON state programming. Based on the simulated results obtained for the R_{ON} variation with $V_{S,NSW}$ after considering multiple values for V_{FGR} and the R_{ON} measured plot, all gathered in Fig. 7.22, the estimated 6.3V for V_{FGR} when VPP=18V (see Tab. 7.3) is confirmed.

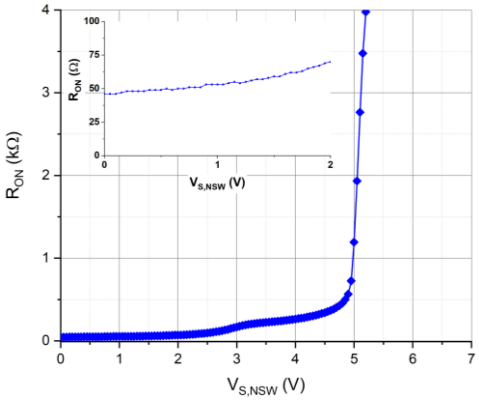


Fig. 7.8 *Measured R_{ON} variation with $V_{S,NSW}$ [23].*

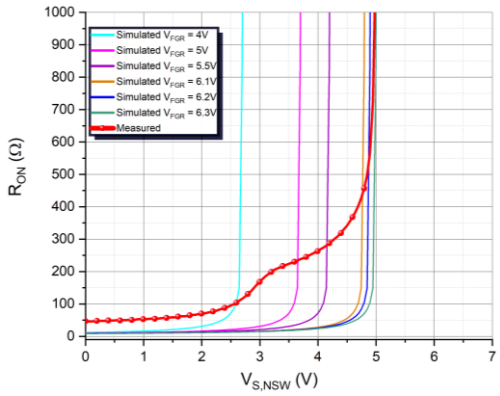


Fig. 7.9 *R_{ON} variation with $V_{S,NSW}$. The red curve corresponds to the measured variation, while all other curves correspond to the simulated variations obtained for different V_{FGR} [23].*

The OFF state was confirmed by the small leakage current of maximum 5nA measured after the OFF-programming sequence was applied.

There was also proposed a bidirectional version of the nonvolatile switch working on the same principle, but this version was not implemented in silicon.

7.3 Conclusions

Within this chapter there were proposed two new switch configurations with superior performances to those studied by simulations in chapter 5.

These new configurations eliminate actual limitations of digital potentiometers caused by standard switches. The first one concerns the maximum voltage that can be applied on the potentiometer endings which is currently limited to the supply voltage. This is caused by the inability of applying voltages higher than the supply on the switch. Both proposed switches ensure correct operation when the applied voltage exceeds the supply range as long as it remains under transistor maximum operating voltage or under the programmed command voltage.

Moreover, the second described configuration, the nonvolatile switch, diminishes the dependency of the digital potentiometers' performances on the supply voltage which is so constraining in low-voltage applications. An ideal example of application that would benefit from all advantages brough by the nonvolatile switch is the hearing aid. The actual employed solution uses charge pumps to provide enough voltage levels for the switches gate command voltages. These charge pumps introduce unwanted noise and consume a lot to keep the switch state. The use of nonvolatile switches in hearing aids would eliminate the noise issue, would offer small on-resistances for voltages under 2V (maximum battery supplied voltage limit), would reduce a lot the power consumption and would not need separate memory blocks for storing the potentiometer step when powered off.

Chapter 8

Conclusions

8.1 Obtained results

The doctoral thesis covers digitally programmable potentiometers (DPPs). In particular it presents schematic and layout designs, silicon implementations, simulations, electrical measurements, comparisons between simulated and experimental results and new mathematical models developed for the digital potentiometers.

In the beginning, in chapter 2, the doctoral thesis presents the DPP internal structure, its characteristic parameters and typical applications. A digital potentiometer consists of two main sections: the digital control section responsible with the adjustment of the second part, the potentiometer itself (composed of incremental resistors and switches). Both sections were analyzed throughout the thesis, but improvements were brought only to the potentiometer section. This is the DPP part on which most of the parameters depend. The performance requirements in the audio-video systems (most usual applications of DPP) concern as small as possible consumed area, reduced working voltages and power consumption, but also the ability of ensuring fine and uniform/linear tuning.

In the third chapter, the digital section of a DPP was discussed. The I^2C digital interface was considered since it is the most common way of synchronous communicating between the digital potentiometer and the user. Based on a particular case of a complex DPP, functionality simulations results corresponding to the most common operations that can be done through the I^2C interface were shown.

Within chapter 4, 12 potentiometers configurations selected from the literature were presented. Here were exposed 11 multistage architectures from two categories: topologies with bulk resistors (B0-B3) and configurations with binary weighted resistors (BW1-BW7), but also the classical single stage architecture (SS). Each of them was designed in a 0.18µm CMOS technology for an 8-bits resolution and a total resistance of 10kΩ. All 12 configurations were compared through simulations. The investigation done on the consumed area indicated that architectures having binary weighted resistors are the most cost-efficient. As it concerns the introduced errors, the classical approach is the best since it has zero errors, but its drawback is the huge area. The largest errors correspond to configurations with binary weighted resistors. The compromise solution with respect to the consumed area and errors is represented by the architectures built with bulk resistors. For large voltages (5.5V), the B2 configuration is the most recommended since it has small nonlinearity errors (INL<0.05, DNL<0.12) and small area (0.037mm^2). In turn, for low voltages (2.7V),

B3 topology is superior to B2. The DNL error below 0.29LSB is significantly smaller than that obtained for B2 configuration (1.47LSB). The use of B3 architecture instead of B2 comes with the price of a double wiper resistance and slightly larger area ($0.046mm^2$). To conclude, the B2 and B3 configurations offer the best performances with respect to the consumed area and linearity characteristics for the design of high-resolution digital potentiometers. Based on this conclusion, both B2 and B3 architectures were used in the silicon implementation of digital potentiometers. Moreover, two new improved versions (B4 and B4D) were derived from the B2 architecture.

Chapter 5 examined switches, important elements in the potentiometer structure. Their characteristic directly influences DPP performances. The on-resistance dictates the wiper resistance, the minimum supply voltage of the potentiometer, but also the voltage range that can be applied on its endings. Additionally, it influences the errors in the case of the multistage architectures. The bidirectionality facilitates the DPP ending terminals interchange while the off-state leakage current influences the digital potentiometer consumption. Within this chapter various common switches based on MOS transistors were analyzed. The study started with the simplest switch implemented using only one type of transistor (nMOS or pMOS). Then three more complicated versions (CMOS) were exposed. For the nMOS switch both unidirectional and bidirectional schematics were considered. For all other switches only the bidirectional structure was investigated. Each switch was designed and simulated in a 0.18µm CMOS technology considering the criterion of maximum on-resistance of 100Ω for V_{CC}=2.7V. The simulated results had shown that the voltage range that can be applied on the switch while the on-resistance criterion is met is limited for both nMOS (<1.34V) and pMOS (>1.4V) switches. By contrast, CMOS switches respect the on-resistance condition for whole range $0 \div V_{CC}$. For these switches actual techniques were employed for the switching devices substrate biasing. The used mechanisms significantly reduced the consumed area but also the off-state leakage current. In particular, the area was reduced from $5650\mu m^2$ (CMOS I, classical configuration) to about $1600\mu m^2$ for CMOS II and III. As it concerns the I_{OFF} current the 200nA value (CMOS I) was lowered to 22nA (CMOS II and CMOS III).

In chapter 6 two new potentiometers architectures (B4 and B4D) were proposed. The linearity and area performances of these new configurations are superior to all architectures presented in chapter 4. They were derived from the B2 topology and were designed and simulated in similar conditions. Simulated results had shown a significant reduction in the nonlinearity errors compared to B2. For B4 configuration both INL and DNL errors were lowered to 0.015LSB, compared to 0.8LSB (INL) and 1.5LSB (DNL) found for B2 architecture. As it concerns the B4D topology nonlinearity errors, these were reduced even more to maximum 0.0005LSB.

The new B4D architecture, but also B2 and B3 configurations (from chapter 4) were used in the silicon implementation of digital potentiometers having 8-bits of resolution (256 steps) and I^2C interface. For the 50kΩ DPPs there were measured several parameters: the total resistance tolerance and TCR, the wiper resistance (R_W) and the nonlinearity errors variations with the potentiometer step. By comparatively analyzing the measured data resulted that the most stable DPP is that based on B3 architecture. The total resistance tolerance for it is 7% while its TCR is -140ppm/°C. Maximum wiper resistance for V_{CC}=2.7V has the smallest value, 90Ω, for the B3 topology-based DPP and the largest, 325Ω, for the B4D topology-based DPP. For high voltages (5.5V), R_W has the smallest maximum value for the B4D CMOS

implemented architecture. As it concerns the nonlinearity errors, the most performant DPP corresponds to that employing the new B4D configuration. Its maximum absolute nonlinearity errors are situated below 0.3LSB for INL and 0.13LSB for DNL compared to 0.4LSB (both INL and DNL) in the case of the B2 architecture-based DPP and 1LSB (INL) and 1.2LSB (DNL) for the B3 architecture-based DPP. For each of these three configurations mathematical models were proposed for determining the INL and DNL theoretical values. The main purpose was to figure out the factors causing the measured linearity characteristics variations. The experimental nonlinearity errors for the 10kΩ DPP implemented in silicon (in an EEPROM process) using the proposed B4D architecture had shown that the parasitical resistance strongly influences the linearity characteristics of the potentiometer. To conclude, designing a highly linear DPP is conditioned by a compact and matched layout, but also by the chosen architecture and technology.

Within chapter 7 there were exposed two new switches configurations that allow the digital potentiometer endings-applied voltages to be higher than its supply voltage. This is an actual limitation of the DPPs existing on the market. Both configurations were investigated through simulations. The first one, the CMOS switch with extended range over the supply voltage was designed and simulated in the same technology and for the same on-resistance criterion as those switches versions presented in chapter 5. Now the resulted area was 4300μm^2. Compared to CMOS II and III from chapter 5, the new switch area is larger, but still smaller than that of CMOS I. It is also superior to CMOS I with respect to the off-state leakage current (50nA compared to 200nA). Though, the major advantage of the proposed switch is the extended voltage range.

The second switch configuration presented in chapter 7 is the nonvolatile switch. The switching element is now an nMOS floating gate transistor. One of the most remarkable characteristics of this switch is that its applied voltage and its on-resistance are independent of the supply voltage, unlike standard switches. They depend only on the programmable command voltage from the floating gate. The switch state programming is done through a separate memory cell by properly applying programming voltages. Another, distinguishable characteristic is that the nonvolatile switch can retain its state and this allows no power consumption after it gets programmed. The unidirectional version of the nonvolatile switch was designed and implemented in a 0.18μm EEPROM process. Its functionality was proven both by simulations and wafer measurements. Based on the experimental testing resulted that the floating gate can be increased up to a certain point through the rising of the programming voltage value. Additionally, the measured on-resistance of the switch has small values (between 45Ω and 70Ω) for source voltages below 2V. The maximum off-state measured leakage current was 5nA. The small values of the on-resistance, independent on the supply voltage, the small consumed current and its nonvolatile nature emphasize the utility of the nonvolatile switch in the design of nonvolatile DPPs used for the volume adjustments of hearing aids, but also other portable devices.

8.2 Original contributions

The original contributions can be found in all chapters.
1. Literature synthesis concerning:

- digital potentiometers architectures, parameters, applications;
- switches;
- I^2C digital interfaces.

2. Improved circuit architectures for:
   - potentiometers: B4, B4D versions [7];
   - switches: the CMOS switch with extended range over the supply voltage [3] and the nonvolatile switch [2], [5].
3. Silicon implementation of one switch and 4 DPP configurations:
   - the nonvolatile unidirectional switch in 0.18µm EEPROM technology [2];
   - the volatile B2 architecture-based DPP in 0.5µm CMOS technology [8];
   - the nonvolatile B3 architecture-based DPP in 0.5µm EEPROM technology [8];
   - the volatile B4D architecture-based DPP in 0.18µm CMOS technology [7];
   - the nonvolatile B4D architecture-based DPP in 0.18µm EEPROM technology [6].
4. Layout design and drawing for:
   - the nonvolatile unidirectional switch [2], [5];
   - the 4 digital potentiometers implemented in silicon [6].
5. Simulation testing for the functionality and performances of multiple circuit families::
   - potentiometers [1], [4], [6], [7];
   - switches [2], [3], [5].
6. Comparison between experimental and simulated results (for the B4D architecture linearity characteristics and the nonvolatile switch).
7. Mathematical models proposed for determining the INL and DNL errors for three architectures: B2, B3 și B4D CMOS [7]; comparison between the data obtained using these models and experimental results.
8. Layout parasitic resistance influence analysis over the linearity performances of the B4D EEPROM architecture [6].
9. Wafer measurements done on the nonvolatile unidirectional switch [2].
10. Functionality simulations done on the digital control section (I^2C interface) of a DPP

8.3 List of original publications

1. **Ilie (Chiranu), G.-C.**; Tudoran, C.; Neagoe, O.; Brezeanu, G., "*Low Cost Approaches for High Resolution Digitally Programmable Potentiometers*", Romanian Journal of Information Science and Technology (ROMJIST), Vol: 23, 2020, Q4 (IF=0.485), ISI, WOS: 000532321500004.
2. **Ilie (Chiranu), G.-C.**; Tudoran, C.; Neagoe, O.; Drăghici, F.; Brezeanu, G., "*Nonvolatile Analog Switch for Low-Voltage Applications*", Electronics Journal, Volume 10, no. 6: 736, March 20, 2021, Q2 (IF=2.412), ISI, WOS: 000634338200001, DOI: 10.3390/electronics10060736.
3. **Ilie (Chiranu), G.-C.**; Tudoran, C.; Neagoe, O.; Brezeanu, G., "*Improved CMOS Analog Switch*", International Symposium on Signals, Circuits and Systems (ISSCS), June 11-12, Romania, Iasi, 2019, ISI, WOS: 000503459500048, DOI: 10.1109/ISSCS.2019.8801776.

4. **Ilie (Chiranu), G.-C.**; Tudoran, C.; Neagoe, O.; Brezeanu, G., "*Performance Analysis for High Resolution Digitally Programmable Potentiometers*", International Semiconductor Conference (CAS), October 9-11, Romania, Sinaia, 2019, ISI, WOS: 000514295300038, DOI: 10.1109/SMICND.2019.8923775.
5. **Ilie (Chiranu), G.-C.**; Tudoran, C.; Neagoe, O.; Brezeanu, G., "*Nonvolatile Analog Switch*", International Conference on Electronics, Computers and Artificial Intelligence (ECAI), June 25-27, Romania, 2020, ISI, WOS: 000627393500103, DOI: 10.1109/ECAI50035.2020.9223230.
6. **Ilie (Chiranu), G.-C.**; Tudoran, C.; Neagoe, O.; Brezeanu, G., "*Parasitic Resistance Influence on High Resolution Digitally Programmable Potentiometers Linearity*", International Semiconductor Conference (CAS), October 7-9, Romania, 2020, ISI, WOS: , DOI: 10.1109/CAS50358.2020.9268041.
7. **Ilie (Chiranu), G.-C.**; Tudoran, C.; Neagoe, O.; Pristavu, G.; Brezeanu, G, "*Digitally Programmable Potentiometer Multistage Architecture with Switch Independent Linearity*", paper accepted to be presented at the PhD Research in Microelectronics and Electronics (PRIME) conference, 19-22 July, 2021, ISI.
8. **Ilie (Chiranu), G.-C.**; Tudoran, C.; Pristavu, G.; Brezeanu, G., "*8-bit Digitally Programmable Potentiometer Multistage Architectures – Experimental Results*", paper prepared for International Semiconductor Conference (CAS), 6-8 October, 2021, ISI.

8.4 Perspectives for further developments

The future research will be based on the design and silicon implementation of digital potentiometers where the improved proposed switches will be employed.

Moreover, in order to reduce even more the linearity errors of the digital potentiometers using the B4D architecture, layout strategies for minimizing the interconnecting wires and matching the poly resistances will be approached.

As it concerns the digital control section of the digital potentiometer, the new I^3C communication protocol (allowing transfer rates of 12.5MHz) will be considered.

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[18] G.-C. Ilie (Chiranu), C. Tudoran, O. Neagoe, G. Pristavu, G. Brezeanu, "*Digitally Programmable Potentiometer Multistage Architecture with Switch Independent Linearity*", paper accepted for presentation at PhD Research in Microelectronics and Electronics (PRIME) conference, 19-22 July, 2021

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