Low supply, low temperature dependency, CMOS only voltage reference

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Abstract – This paper focuses on design considerations regarding CMOS only voltage references. In order to achieve low supply dependency a pre-regulator structure is used. In order to improve the temperature dependency, a curvature correction circuit is used.

Keywords – voltage reference, regulation, temperature curvature correction

1. Introduction

Voltage reference circuits are one of the most common and largely used building blocks in electronic circuits. A reliable reference enables reliable comparisons results, reliable conversions between analog and digital and in general a good translation between external stimuli and electrical signals.

As the struggle for cost reduction continues, the necessity for technologies that do not require bipolar or even silicon or poly silicon devices has risen.

CMOS only voltage sources have been presented for a long time now, most notable examples are [1], [2] and [3]. Basic concept behind this type of voltage references is matching of a positive coefficient current source with a negative coefficient current source resulting in an overall compensation of the resulting current in respect to temperature.

Two major issues come with current matching approach: first, there is a nonlinear component (usually negative temperature coefficient) for reference current which needs additional compensation; second, subthreshold transistors are very susceptible to supply variations. In order to alleviate this issue we propose a pre-regulator integration and use a regulated voltage for supplying the reference core.

2. Concept presentation

Proposed concept for top schematic is presented in figure 1.

Fig. 1. Top schematic

Coarse reference block consists from a simple regulator, using a PMOS transistor as a pass device.

Fine reference block consist from a start-up circuit, a reference core (MOS only), and a second order compensation for nonlinear components.

3. Voltage regulator

Proposed concept for voltage regulator is presented in figure 2.

Fig. 2. Voltage regulator schematic

The role of this sub-block is to provide a stable voltage as a supply for the voltage reference core.

Basic equation this block is:
\[ V_{\text{reg, sup}} = V_{\text{REF}} \cdot \frac{(R_1 + R_2)}{R_2} \]  

(1)

A target for this parameter is not the actual value (considered at 4.6V here); only it’s stability with “noisy” supply voltage.

4. Reference voltage schematic

Proposed concept for reference generation block is presented in figure 3.

Points (a) and (b) are kept at the same potential due to operational amplifier. Currents \( I_1 \) and \( I_2 \) are equals due to current mirror formed from \( M_3 \) and \( M_4 \). If \( R_1 \) and \( R_3 \) are equal, we have:

\[ I_{1a} = I_{2a} \]  

(2)

If \( M_1 \) and \( M_2 \) are in subthreshold region we have the following equation:

\[ V_{GS2} - V_{GS1} = aV_T \ln n \]  

(3)

From this we derive the value for \( I_{2a} \) current:

\[ I_{2a} = \frac{1}{R_2} aV_T \ln n \]  

(4)

Where \( V_T \) is the thermal voltage (\( V_T = \frac{kT}{q} \)). As \( V_T \) is proportional with temperature, \( I_{2a} \) is proportional with temperature (PTAT type current).

For CTAT type of current we have to consider again the subthreshold region for gate source voltages of \( M_1 \) and \( M_2 \) [4]:

\[ V_{GS1}(T) = V_{th}(T) + [V_{GS1}(T_o) - V_{th}(T_o)] \frac{T}{T_o} + \frac{akT}{q} (\alpha + m - 2) \ln T \]  

\[ \frac{T_o}{T} \]  

(5)

\[ V_{GS2}(T) = V_{th}(T) + [V_{GS2}(T_o) - V_{th}(T_o)] \frac{T}{T_o} + \frac{akT}{q} (\alpha + m - 2) \ln T \]  

\[ \frac{T_o}{T} \]  

(6)

where \( \alpha = 1 \) (\( I_{1a}, I_{2a} \) are PTAT type currents)

Currents \( I_{1b} \) and \( I_{2b} \) can be written as:

\[ I_{1b} = I_{2b} = \frac{V_{GS2}}{R_2} = \frac{1}{R_2} \left[ V_{th}(T) + [V_{GS2}(T_o) - V_{th}(T_o)] \right] \cdot \frac{T}{T_o} + \frac{akT}{q} (\alpha + m - 2) \ln T \]  

\[ \frac{T_o}{T} \]  

(7)

Combining equations (3) and (6) we obtain:

\[ I_{2a} + I_{2b} = I_{2\text{CTAT}} + I_{2\text{PTAT}} + I_{2\text{NL}} = I_{\text{REF}} \]  

(8)
Current $I_{\text{REF}}$ together with resistor $R_4$ create the voltage reference. Component $I_{\text{PTAT}}$ is proportional with temperature, $I_{\text{CTAT}}$ is complementary with temperature variations and $I_{\text{NL}}$ is a current which decrease non-linear with the temperature; for it’s compensation a 2nd order compensation schematic will be used. In detail, for each component, we have:

$$I_{\text{CTAT}} = \frac{V_{T_h}(T)}{R_1} \quad (9)$$

$$I_{\text{PTAT}} = T \cdot \left( \frac{1}{R_1} \frac{V_{\text{GS}2}(T_o) - V_{\text{Th}}(T_o)}{T_o} + \frac{1}{R_2} \frac{ak}{q} \ln n \right) \quad (10)$$

$$I_{\text{NL}} = \frac{akT}{qR_1} (m-1) \ln \frac{T}{T_o} \quad (11)$$

### 6. 2nd order compensation schematic

Proposed concept for nonlinear component compensation block is presented in figure 5.

![Fig. 5. PTAT^2 current generator](image)

For this schematic we can write the following equations:

$$V_{\text{GS}1} + V_{\text{GS}2} = V_{\text{GS}4} + V_{\text{GS}3} \quad (12)$$

this translate to (in hypotesys that all transistor are equal):

$$2V_{\text{GS}}(I_o) = V_{\text{GS}}(I'_\text{OUT} - I_{\text{IN}}) + V_{\text{GS}}(I'_\text{OUT}) \quad (13)$$

where $V_{\text{GS}}(I)$ is gate source voltage of a MOS transistor at current $I$.

Equation (13) is equivalent to:

$$2\sqrt{I_o} = \sqrt{I_{\text{OUT}} - I_{\text{IN}}} + \sqrt{I_{\text{OUT}}} \quad (14)$$

Combining this with:

$$I_{\text{OUT}} = I_{\text{OUT}} + I_o + \frac{I_{\text{IN}}}{2} \quad (15)$$

We obtain:

$$I_{\text{OUT}} = \frac{I_o^2}{16} \cdot \frac{1}{I_o} \quad (16)$$

This current is a $\text{PTAT}^2$ current is assumption that $I_{\text{IN}}$ is a PTAT current and $I_o$ is a constant current with the temperature.

### 7. Implementation and simulation results

For implementation we have use a 2um CMOS technology, with no special requirements. The schematic concept is easy adaptable, no special components are required.

Top schematic is presented in figure 6, regulator schematic is presented in figure 7, reference voltage sub-top is presented in figure 8.

![Fig. 6. Top schematic](image)

![Fig. 7. Voltage regulator schematic](image)
Simulations results across technological corners, temperature range (-40° to 150°C) show an overall variation between 1.21 V to 1.32 V with a nominal value of 1.256 V. This gives an overall error of 5.01% error, giving this reference circuit a slight worse precision than a normal bandgap circuit constructed using silicon diodes.

A start-up – shutdown sequence is presented in figure 9.

A layout implementation is presented in figure 10.

8. Conclusions
This paper presents a simple, cost efficient alternative to classical bandgap voltage references, using only CMOS transistors and poly silicon resistors. A “classical” CMOS only reference with additional regulation of internal supply voltage was proposed solution. In order to compensate higher order non-linearity of reference current additional compensation was added.

The simulation results shows a good match to theoretical model, overall result shows a small relative error in respect to technology, temperature and supply voltage.

References